

(19)



(11)

EP 4 682 670 A1

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
21.01.2026 Bulletin 2026/04

(51) International Patent Classification (IPC):
G05F 3/24 (2006.01) G05F 3/30 (2006.01)

(21) Application number: **24188848.6**

(52) Cooperative Patent Classification (CPC):
G05F 3/30; G05F 3/242

(22) Date of filing: **16.07.2024**

(84) Designated Contracting States:
**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HR HU IE IS IT LI LT LU LV MC ME MK MT NL
NO PL PT RO RS SE SI SK SM TR**
Designated Extension States:
BA
Designated Validation States:
GE KH MA MD TN

(71) Applicant: **BIOTRONIK SE & Co. KG**
12359 Berlin (DE)

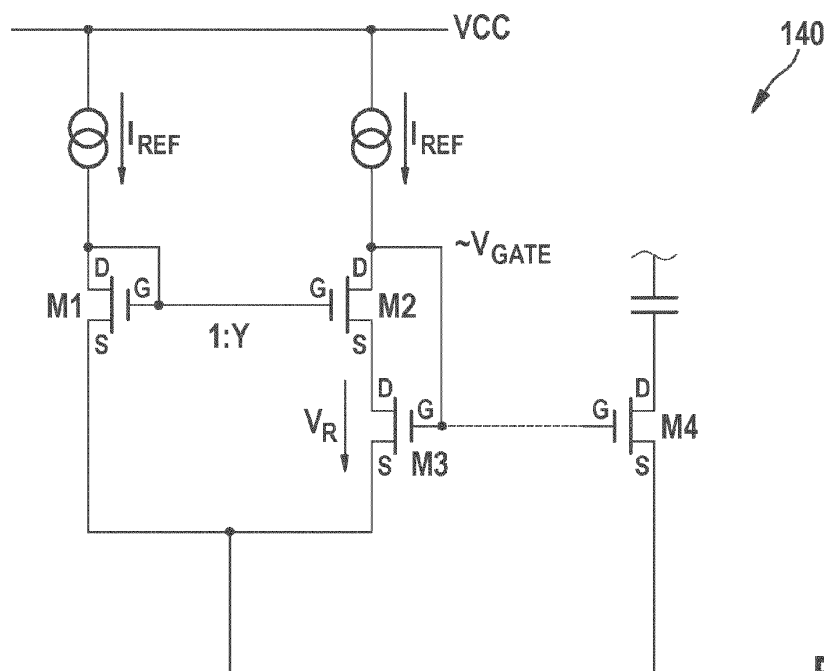
(72) Inventor: **Wiesheier, Markus**
96114 Hirschaid (DE)

(74) Representative: **Biotronik Corporate Services SE**
Corporate Intellectual Property
Sieversufer 7-9
12359 Berlin (DE)

(54) CIRCUIT ARRANGEMENT FOR USE IN AN IMPLANTABLE MEDICAL DEVICE

(57) A circuit arrangement (140-144) for use in an implantable medical device (1) is configured for providing a temperature-compensated output resistance and comprises a first MOSFET transistor (M3), a first circuit portion configured to supply a temperature-dependent reference current (I_{REF}) to the first MOSFET transistor (M3), and a second circuit portion configured to generate

a temperature-dependent output voltage (V_R) across a drain (D) and a source (S) of the first MOSFET transistor (M3), such that an ON resistance ($R_{ON,M3}$) of the first MOSFET transistor (M3) resulting from the output voltage (V_R) and the reference current (I_{REF}) provides the temperature-compensated output resistance.

**FIG. 2**

Description

[0001] The instant invention relates to a circuit arrangement for use in an implantable medical device and to an implantable medical device comprising such a circuit arrangement.

[0002] A circuit arrangement of this kind is configured for providing a temperature-compensated output resistance.

[0003] A circuit arrangement of this kind shall be employed in a processing circuitry of an implantable medical device. An implantable medical device of this kind may for example be a cardiac stimulation device, such as a cardiac pacemaker device or a cardiac defibrillator device. For example, the implantable medical device is a cardiac resynchronization therapy device (CRT), for example comprising a defibrillation function (CRT-D). In another embodiment, the implantable medical device is an implantable cardioverter defibrillator (ICD). In yet another embodiment, the implantable medical device is an implantable neuro-stimulation device, an implantable sensor device such as a pressure sensing device, or an implantable monitoring device such as a bio-monitor for monitoring and recording signals within a patient.

[0004] Generally, implantable medical devices, such as implantable stimulation devices, shall be small in size and shall be configured for operating within a patient for a prolonged period of time. A processing circuitry of an implantable medical device hence shall operate in a power-efficient manner to allow for a continuous operation in an implanted state, despite strict space constraints imposed on a device battery.

[0005] Analog integrated circuits within a processing circuitry of an implantable medical device typically are implemented using a CMOS analog circuit design employing (p-channel or n-channel) MOSFET transistors. CMOS analog circuit design allows for a design of analog integrated circuits by modelling analog circuit components such as resistances or inductances by an arrangement of MOSFET transistors in a power-efficient and at the same time space-efficient and or area-efficient manner.

[0006] In particular within the design of circuits for use in an implantable medical device, space efficiency is of importance. In addition, when for example designing a resistance in CMOS technology, it is desirable to be able to provide large resistance values which are substantially temperature independent, taking into account that within a patient temperature conditions typically are substantially different than outside of the patient and may vary within the patient.

[0007] For example, when designing a circuit to be used in a communication circuitry for establishing a communication between the implantable medical device and an external device, a resistance in combination with a capacitance is generally required to provide for a filtering circuit in order to tune the communication circuitry to a desired frequency band. For this, in order to allow for a frequency-stable operation, a temperature stability of the resistance is desirable.

[0008] Current approaches for designing a resistance using CMOS technology, for example by using so-called poly-resistances, may suffer from comparatively large space or area requirements or do not allow for a satisfactory temperature compensation.

[0009] It is an object of the instant invention to provide a circuit arrangement and an implantable medical device using such circuit arrangement which allow for a temperature-compensated operation.

[0010] This object is achieved by means of a circuit arrangement comprising the features of claim 1.

[0011] Accordingly, a circuit arrangement for use in an implantable medical device is configured for providing a temperature-compensated output resistance and comprises a first MOSFET transistor, a first circuit portion configured to supply a temperature-dependent reference current to the first MOSFET transistor, and a second circuit portion configured to generate a temperature-dependent output voltage across a drain and a source of the first MOSFET transistor, such that an ON resistance of the first MOSFET transistor resulting from the output voltage and the reference current provides the temperature-compensated output resistance.

[0012] The circuit arrangement comprises a first MOSFET transistor, a first circuit portion and a second circuit portion. The first circuit portion, during operation of the circuit arrangement, supplies a temperature-dependent reference current to the first MOSFET transistor, in particular to the drain of the first MOSFET transistor. The second circuit portion, in turn, generates a temperature-dependent output voltage across the first MOSFET transistor, namely a drain-source voltage across the drain and the source of the first MOSFET transistor. If the temperature dependency of the reference current and the temperature dependency of the output voltage are substantially equal, the temperature dependency of the reference current and the temperature dependency of the output voltage cancel each other out at the first MOSFET transistor, such that an ON resistance of the first MOSFET transistor results which is substantially temperature independent and hence yields a temperature-compensated output resistance.

[0013] The ON resistance of the first MOSFET transistor is computed by dividing the voltage across the drain and the source of the first MOSFET transistor, namely the temperature-dependent output voltage provided by the second circuit portion, by the current flowing from drain to source, imposed by the temperature-dependent reference current. If the temperature dependency of the reference current and the temperature dependency of the output voltage are substantially equal, the temperature dependencies will substantially cancel out, such that a temperature-independent ON resistance results, yielding the temperature-compensated output resistance.

[0014] In one embodiment, the first MOSFET transistor is configured to operate in a linear region of MOSFET operation. Generally, to operate in the linear region, the drain-source voltage is smaller than a saturation voltage. In the linear region

the drain current (at least on a small scale) linearly depends on the drain-source voltage (in comparison to the saturated region, in which the drain current substantially is independent of the drain-source voltage).

[0015] To operate in the linear region, the first MOSFET transistor shall be dimensioned such that its saturation voltage is larger than the output voltage supplied by the second circuit portion in order to ensure an operation in the linear region.

[0016] Operation in the linear region is well-known in CMOS technology and is described in detail for example in the textbook by Phillip E. Allen and Douglas R. Holberg, "CMOS analog circuit design", 1987, ISBN 0-19-510720-9.

[0017] In one embodiment, the temperature-dependent reference current comprises a first temperature dependency and the temperature-dependent output voltage comprises a second temperature dependency, wherein the first temperature dependency and the second temperature dependency are at least approximately equal. In that the reference current as provided by the first circuit portion of the circuit arrangement and the output voltage as generated by the second circuit portion of the circuit arrangement comprise a substantially equal temperature dependency, the temperature dependencies of the reference current and the output voltage cancel out at the first MOSFET transistor, such that the first MOSFET transistor exhibits a substantially temperature-independent ON resistance, providing the temperature-compensated output resistance. In particular, the gate voltage of the first MOSFET transistor will automatically regulate itself such that the ON resistance determined by the drain-source resistance is set according to the reference current supplied to the first MOSFET transistor and the output voltage applied across the drain and the source.

[0018] In one embodiment, the second circuit portion comprises a pair of second MOSFET transistors, wherein gates of the second MOSFET transistors are connected to each other. The second MOSFET transistors are connected to one another such that the output voltage is generated and is applied across the drain and the source of the first MOSFET transistor.

[0019] The value of the output voltage, corresponding to a difference voltage (delta voltage) of the source potentials of the second MOSFET transistors, depends on the dimensions of the second MOSFET transistors, namely a channel width and a channel length of each of the second MOSFET transistors.

[0020] In one embodiment, the second MOSFET transistors are dimensioned with equal channel width W divided by channel length L , $W/L=Y$. Factor $1.Y$ is produced via a multiplier.

[0021] In one embodiment, the second MOSFET transistors are configured to operate in a weak inversion region of MOSFET operation. Generally, in the weak inversion region the gate-source voltage of the second MOSFET transistors is smaller than a threshold voltage associated with the respective MOSFET transistor. Operation in the weak inversion region generally can be ensured by properly dimensioning the second MOSFET transistors, in particular the channel width and channel length of the second MOSFET transistors. Generally, the second MOSFET transistors are dimensioned to be large such that a small gate-source voltage results.

[0022] Operation in the weak inversion region is well-known in CMOS technology and is described in detail for example in the textbook by Phillip E. Allen and Douglas R. Holberg, "CMOS analog circuit design", 1987, ISBN 0-19-510720-9.

[0023] In one embodiment, the first circuit portion is connected to drains of the second MOSFET transistors to supply the reference current to the drains of the second MOSFET transistors. The first circuit portion, which in operation supplies the temperature-dependent reference current, hence is connected to the drains of the second MOSFET transistors in order to feed the temperature-dependent reference current alike into the second MOSFET transistors. The temperature-dependent reference current hence is imposed on the second MOSFET transistors, which hence each comprise a drain-source current as set by to the reference current.

[0024] In one embodiment, the drain of one of the second MOSFET transistors is connected to a gate of the first MOSFET transistor. The drain of the respective second MOSFET transistor generally is in a high-ohmic state. The drain of the second MOSFET transistor is connected to the gate of the first MOSFET transistor, such that the drain of the respective second MOSFET transistor and the gate of the first MOSFET transistor are at equal potential.

[0025] In one embodiment, the source of said one of the second MOSFET transistors is connected to the drain of the first MOSFET transistor. The source of the first MOSFET transistor is connected for example to ground, or may be connected to a voltage source or another MOSFET transistor in order to provide for a voltage shift at the source of the first MOSFET transistor. The first MOSFET transistor hence is arranged in between the source of the respective one of the second MOSFET transistors and ground (or a voltage source or another MOSFET transistor in the path towards ground).

[0026] In one embodiment, the drain and the gate of the other of the second MOSFET transistors are connected to each other. The drain and the gate of the other of the second MOSFET transistors hence are short-circuited and are at the same potential. The second MOSFET transistors together provide for the voltage corresponding to a difference voltage (delta voltage) in between the sources of the two second MOSFET transistors. Said voltage can be the output voltage, or generating the output voltage with other voltage sources or another MOSFET transistor in the path toward ground.

[0027] In one embodiment, the first circuit portion comprises a pair of third MOSFET transistors. The gates of the third MOSFET transistors are connected to each other, such that the gates of the third MOSFET transistors are at equal potential.

[0028] In one embodiment, the third MOSFET transistors are configured to operate in a weak inversion region of MOSFET operation. For this, the first circuit portion is operated such that the gate-source voltage of both of the third

MOSFET transistors is smaller than a threshold voltage associated with the respective MOSFET transistor. In order to ensure an operation in the weak inversion region, the third MOSFET transistors may for example be dimensioned large, i.e. to comprise a comparatively large channel width and length.

[0029] In one embodiment, the first circuit portion comprises a pair of fourth MOSFET transistors connected at their gates and serving as a current mirror. The pair of fourth MOSFET transistors is connected to the pair of third MOSFET transistors such that a drain of each of the fourth MOSFET transistors is connected to a drain of one of the third MOSFET transistors. In that the pair of fourth MOSFET transistors functions as a current mirror, an equal current is passed through the pair of third MOSFET transistors.

[0030] According to an embodiment, the pair of fourth MOSFET transistors are p-type MOSFET transistors, or PMOS transistors, wherein the pair of first, second and third MOSFET transistors are NMOS transistors. The pair of fourth MOSFET transistors have the source on the V_{cc} side. The voltages from source to drain and from source to gate are of positive polarity.

[0031] According to an embodiment, the drain of one of the MOSFET transistors from the pair of fourth MOSFET transistors and the connected drain of one of the third MOSFET transistors are connected to a third circuit portion. The third circuit portion comprises a pair of fifth MOSFET transistors connected at their gates and serving as a current mirror. In that the pair of fifth MOSFET transistors functions as a current mirror, an equal current, for instance a reference current I_{REF} , is passed through the pair of fifth MOSFET transistors.

[0032] According to an embodiment, the pair of fifth MOSFET transistors are PMOS transistors, having the source on the V_{cc} side. The voltages from source to drain and from source to gate are of positive polarity.

[0033] In one embodiment, the MOSFET transistors of the pair of fifth MOSFET transistors are dimensioned with equal channel width W divided by channel length L, as the W/L of one MOSFET transistor of the pair of fourth MOSFET transistors.

[0034] In one embodiment, one of the third MOSFET transistors at its source is connected to a non-temperature-dependent resistance. The first circuit portion is configured to output the reference current according to a reference voltage produced across the non-temperature-dependent resistance. The reference voltage is produced as a difference voltage (delta voltage) between the pair of third MOSFET transistors and comprises a temperature dependency in accordance with the temperature dependency of the third MOSFET transistors. In that the reference voltage is applied across the non-temperature-dependent reference resistance, the reference current results which exhibits a temperature dependency according to the temperature dependency of operation of the third MOSFET transistors.

[0035] Whereas the temperature dependency of the first circuit portion for providing the temperature-dependent reference current is largely governed by the pair of third MOSFET transistors, the temperature dependency of the second circuit portion for providing the temperature-dependent output voltage is largely governed by the pair of second MOSFET transistors. By suitably choosing the third MOSFET transistors and the second MOSFET transistors, thus, a substantially equal temperature dependency of both the first circuit portion and the second portion may be achieved, such that a temperature compensation may be obtained by a cancellation of the temperature dependency of the reference current and the temperature dependency of the output voltage.

[0036] In one embodiment, the gate of the first MOSFET transistor is connected to a gate of a target (MOSFET) transistor to produce a temperature-independent ON resistance at the target transistor. The first MOSFET transistor in particular may function as a reference to control any target MOSFET transistor to obtain a substantially constant (temperature-independent) ON resistance. By connecting one or multiple target transistors to the first MOSFET transistor, a controlling of the gate of multiple target transistors may be established for controlling the ON resistance of the target transistors to be substantially temperature-independent.

[0037] In one embodiment, an implantable medical device for performing a therapeutic and/or diagnostic function in a patient comprises a circuit arrangement of the kind described above. The implantable medical device in particular may be a stimulation device, such as a cardiac stimulation device or a neuro-stimulation device. For example, the implantable medical device may be a cardiac pacemaker device or a cardiac defibrillator device, such as a CRT device or an ICD device. In other embodiments, the implantable medical device may for example be an implantable sensor device or an implantable monitoring device.

[0038] The various features and advantages of the present invention may be more readily understood with reference to the following detailed description and the embodiments shown in the drawings. Herein,

Fig. 1 shows a schematic drawing of a system comprising an implantable medical device implanted in a patient;

Fig. 2 shows a circuit schematic of a circuit arrangement for providing a temperature-compensated output resistance at a target transistor;

Fig. 3 shows a circuit schematic of a first circuit portion of the circuit arrangement for providing a temperature-dependent reference current;

Fig. 4 shows a circuit schematic of another embodiment of a circuit arrangement for providing a temperature-compensated output resistance;

Fig. 5 shows a circuit schematic of yet another embodiment of a circuit arrangement for providing a temperature-compensated output resistance;

Fig. 6 shows an output characteristic of a MOSFET device; and

Fig. 7 shows a characteristic indicating the three regions of operation of a MOSFET transistor.

[0039] Subsequently, embodiments of the invention shall be described in detail with reference to the drawings. In the drawings, like reference numerals designate like structural elements.

[0040] It is to be noted that the embodiments are not limiting for the invention, but merely represent illustrative examples.

[0041] Referring to Fig. 1, in one embodiment a system comprises an implantable medical device 1 implanted into a patient for serving a therapeutic cardiac stimulation function. The implantable medical device 1, in the shown embodiment, comprises a generator device 10 and an arrangement of electrode leads 11, 12, 13 extending from the generator device 10. The generator device 10 may for example be implanted subcutaneously into a patient P, the electrode leads 11, 12, 13 reaching into the patient's heart for monitoring cardiac activity of the patient's heart.

[0042] The generator device 10 comprises a processing circuitry 14 encapsulated in a housing of the generator device 10 together with an electrochemical battery for supplying electrical energy for operation of the implantable medical device 1.

[0043] The system furthermore comprises an external device 2 external to the patient P and being in communication connection with the implantable medical device 1. The external device 2 may be in connection, via a public communication network 4, with a remote server device 3, for example a home monitoring service center (HMSC) accessible by a physician, in the context of a home monitoring system. According to an embodiment, another type of external device (not depicted) is used to communicate with the implantable medical device 1 using a first communication coil in the external device and a second communication coil in the implantable medical device. The external device is brought in proximity (about 10 cm) to the implantable medical device 1 to achieve inductive coupling between the two coils, enabling data exchange. The receiver circuit in the implantable medical device 1 for said coil communication is limited in space and area, and exposed to temperature variations. Using the circuit arrangement(s) of the present invention, resistances can be generated which are constant in regard to with temperature changes and processing variations. The described circuit arrangement(s) can be used for telemetry integrated circuits of implantable medical device 1.

[0044] Generally, the processing circuitry 14 is configured for providing a therapeutic and/or diagnostic function using the implantable medical device 1. In addition, the processing circuitry 14 may be embodied to establish a communication connection to an external device 2 and for this may comprise circuitry in order to establish a communication for example using RF signals.

[0045] The implantable medical device 1, for example a cardiac stimulation device such as a pacemaker device or a defibrillator device, for example a CRT device or an ICD device, generally shall be designed such that it may rest within a patient P over a prolonged duration of time, making it necessary for the implantable medical device 1 to function in an energy-efficient manner by using energy resources of a battery encapsulated within a housing of the implantable medical device 1. As severe space restrictions exist for components of the implantable medical device 1, including the processing circuitry 14 and the battery, it is important to design the implantable medical device 1 with components allowing for a space-efficient implementation of the implantable medical device 1 and at the same time for a power-efficient operation of the implantable medical device 1 over its lifetime.

[0046] The processing circuitry 14 generally, in order to provide for a power-efficient operation and space-efficient structure, is designed using CMOS analog circuit design. In particular, components of the processing circuitry 14, such as resistances or inductances, may be modeled using arrangements of MOSFET transistors.

[0047] Referring now to Fig. 2, in one embodiment a circuit arrangement 140 of the processing circuitry 14 is configured for setting an output resistance at the target transistor M4. The output resistance is set at the target transistor M4 by controlling the gate voltage at the gate G of the target transistor M4 and shall be such that it is substantially temperature independent in order to provide for a temperature-stable resistance.

[0048] Resistances in the processing circuitry 14 may serve different purposes. For example, a resistance may be combined in a communication circuitry with a capacitance in order to provide for a filtering circuit to tune the communication circuitry to a desired frequency band of communication. For this, a temperature-stable operation is desired to allow for a stable communication in a specific, for example narrow frequency band, taking into account that within a patient P temperature conditions are substantially different than outside of the patient P and in addition may vary over time.

[0049] Using the circuit arrangement 140 according to Fig. 2, a temperature-compensated output resistance is set at a MOSFET transistor M3 and also at the target transistor M4 by controlling the gate voltage at the gate G of the target

transistor M4 using the MOSFET transistor M3.

[0050] Namely, the circuit arrangement 140 according to Fig. 2 comprises a first circuit portion configured for delivering a reference current I_{REF} , denoted in Fig. 2 by current sources and shown in an embodiment in Fig. 3.

[0051] In addition, the circuit arrangement 140 according to Fig. 2 comprises a second circuit portion made up of MOSFET transistors M1, M2, which are fed at their drains D with the reference current I_{REF} and are connected to one another at their gates G. One of the MOSFET transistors M1, M2 - in the example of Fig. 2 the MOSFET transistor M2 - at its source S is connected to the drain D of the MOSFET transistor M3. In addition, the drain D of the MOSFET transistor M2 is connected to the gate G of the MOSFET transistor M3, such that the gate voltage V_{gate} of the MOSFET transistor M3 is drawn to the high-ohmic drain D of the MOSFET transistor M2. Further, the drain D of the MOSFET transistor M1 is connected (short-circuited) to its gate G.

[0052] Generally, any MOSFET transistor as concerned herein comprises a drain D, a source S and a gate G as well-known in the art and as typical for a MOSFET transistor.

[0053] Using the second circuit portion comprising the MOSFET transistors M1, M2, an output voltage V_R is applied across the drain D and the source S of the MOSFET transistor M3, as it is indicated in Fig. 2. The output voltage V_R herein is provided as a difference voltage (delta voltage) in between the sources S of the MOSFET transistors M1, M2.

[0054] The MOSFET transistors M1, M2 operate in a weak inversion region of MOSFET operation. As it is well-known in MOSFET technology, in the weak inversion region WI as illustrated in the characteristic of Fig. 7 the gate-source voltage is below a threshold voltage (generally denoted as V_T in the literature), whereas in contrast in a strong inversion region SI, separated from the weak inversion region WI by a moderate inversion region MI, the gate-source voltage is above the threshold voltage. This is described in detail e.g. in the textbook by Phillip E. Allen and Douglas R. Holberg, "CMOS analog circuit design", 1987, ISBN 0-19-510720-9.

[0055] The MOSFET transistor M3, in turn, operates in the linear region, in which the drain-source voltage is below a saturation voltage, as it is indicated in Fig. 6 and as it is commonly known in MOSFET technology.

[0056] The output voltage V_R for the MOSFET transistors M1, M2 operating in the weak inversion region can be computed as follows:

$$V_R = V_{Temp} * \ln(Y) \quad (1)$$

where V_{Temp} is a temperature voltage equal to

$$V_{Temp} = \left(\frac{k_B * T}{e} \right) \approx 26.7 \text{ mV at } 37^\circ\text{C} \quad (2)$$

(k_B : Boltzmann constant; T : absolute temperature in Kelvin; e : elementary charge) and Y is a factor computed according to the ratio of channel width W and channel length L of the two MOSFET transistors M1, M2 as follows:

$$Y = \frac{\left(\frac{W}{L} \right)_{M2}}{\left(\frac{W}{L} \right)_{M1}} \quad (3)$$

[0057] The output resistance at the MOSFET transistor M3 corresponds to the ON resistance $R_{ON,M3} = R_{DS,M3}$ of the MOSFET transistor M3, which is computed as follows:

$$R_{DS,M3} = R_{ON,M3} = \frac{V_R}{I_{REF}} \quad (4)$$

[0058] As visible from equation (1) above, the output voltage V_R comprises a temperature dependency according to the temperature voltage V_{Temp} . In addition, in the circuit arrangement 140 according to Fig. 2 the reference current I_{REF} is provided to comprise a temperature dependency which at least is similar to the temperature dependency of the output voltage V_R , such that according to equation (4) the temperature dependencies cancel each other out, and a substantially constant output resistance $R_{ON,M3} R_{DS,M3}$ results.

[0059] In one embodiment, the reference current I_{REF} is provided by a circuit portion 141 as illustrated in the circuit schematic of Fig. 3.

[0060] The circuit portion 141 according to Fig. 3 comprises a pair of MOSFET transistors M5, M6, which are connected to each other at their gates G. A pair of further MOSFET transistors M7, M8, which are PMOS transistors, have the source on the V_{cc} side. The voltages from source to drain and from source to gate are of positive polarity. M7, M8 function as a

current mirror and is formed equal, the MOSFET transistors M7, M8 being connected at their sources S to a supply voltage VCC and at their drains D to the drains D of the MOSFET transistors M5, M6, as this is shown in Fig. 3. The gate G of the MOSFET transistor M8 herein is connected (short-circuited) to its drain D. The drain D of the MOSFET transistor M5 is connected (short-circuited) to its gate G.

[0061] According to an embodiment, the drain of M8 and the drain of connected M6 are connected to another circuit portion 144. The circuit portion 144 comprises a pair of MOSFET transistors M11, M12 which are connected at their gates and serving as a current mirror. In that the pair of MOSFET transistors M11, M12 functions as a current mirror, an equal current, for instance a reference current I_{REF} , is passed through the pair of MOSFET transistors M11, M12.

[0062] According to an embodiment, the pair of MOSFET transistors M11, M12 are PMOS transistors, having the source on the Vcc side. The voltages from source to drain and from source to gate are of positive polarity.

[0063] In one embodiment, the MOSFET transistors of M11, M12 are dimensioned with equal channel width W divided by channel length L, as the W/L of one MOSFET transistors M8 or M9, for example M8.

[0064] In that the MOSFET transistors M7, M8 function as a current mirror with factor 1:1 or other factors, they impose an identical reference current I_{REF} through the MOSFET transistors M5, M6, such that the drain currents of both MOSFET transistors M5, M6 are equal and correspond to the reference current I_{REF} .

[0065] The MOSFET transistor M6 at its source S is connected to a reference resistance R_{REF} which comprises a substantially temperature-independent, constant resistance.

[0066] The MOSFET transistors M5, M6 both operate in the weak inversion region.

[0067] The reference voltage V_{REF} across the reference resistance R_{REF} is computed as follows:

$$V_{REF} = V_{Temp} * \ln\left(\frac{I_{D,M5}}{I_{D,M6}} X\right) \quad (5)$$

where V_{Temp} again is the temperature voltage, and X is a factor according to

$$X = \frac{\left(\frac{W}{L}\right)_{M6}}{\left(\frac{W}{L}\right)_{M5}} \quad (6)$$

W, L represent the channel width and the channel length of the respective transistor M5, M6, such that the factor X expresses the ratio of channel width and channel length of the two transistors M5, M6.

[0068] As the current through the MOSFET transistors M5, M6 is equal ($I_{D,M5} = I_{D,M6}$) and corresponds to the reference current I_{REF} imposed by the current mirror of the pair of MOSFET transistors M7, M8, the reference voltage becomes

$$V_{REF} = V_{Temp} * \ln(X) \quad (7)$$

and the reference current is

$$I_{REF} = \frac{V_{REF}}{R_{REF}} = \frac{V_{Temp}}{R_{REF}} * \ln(X) \quad (8)$$

[0069] When applying equation (8) to equation (4), the output resistance corresponding to the ON resistance of the MOSFET transistor M3 in the circuit arrangement 140 of Fig. 2 becomes, when assuming a linear characteristic curve,

$$R_{DS,M3} = R_{ON,M3} = \frac{V_{REF}}{I_{REF}} = R_{REF} * \frac{\ln(Y)}{\ln(X)} \quad (9)$$

[0070] More exact, the output resistance corresponding to the ON resistance of the MOSFET transistor M3 becomes

$$R_{DS,M3} = R_{ON,M3} = \frac{V_{REF}}{I_{REF}} = R_{REF} * \frac{(Y-1)}{\ln(X)} \quad (10)$$

[0071] In both equations (9) and (10) the output resistance is temperature-compensated, in that the temperature dependencies of the output voltage V_R and the reference current I_{REF} cancel out.

[0072] In particular, the gate voltage of the MOSFET transistor M3 will regulate itself according to the output voltage V_R

and the imposed reference current I_{REF} such that an output resistance, corresponding to the drain-source resistance, results which fulfills the equation (4) above.

[0073] If the output voltage V_R and the reference current I_{REF} have the same temperature characteristic, the temperature dependencies cancel each other out, such that a substantially temperature-independent output resistance at the MOSFET transistor M3 results.

[0074] If in addition the output voltage V_R and the reference current I_{REF} have an equal or no process dependency, the output resistance in addition is independent in this respect.

[0075] The gate voltage of the MOSFET transistor M3 serves as a reference voltage for the target transistor M4 and potential further MOSFET transistors, which shall exhibit a defined, temperature-compensated ON resistance. The controlled gate voltage of the MOSFET transistor M3 thus provides for a compensation of temperature variations in the target transistors M4.

[0076] An adaption of a resistance value may be provided by adjusting the transistor geometry of the respective target transistor M4, wherein the output resistance (ON resistance) is indirectly proportional to the ratio of channel width and channel length.

[0077] According to an embodiment, M1, M2 M5 and M6 are in weak inversion region and in saturation. According to an embodiment, M7, M8 and IREF are saturated, wherein M7 and M8 may be in weak inversion, strong inversion or moderate inversion region.

[0078] According to an embodiment, M3 should be dimensioned so that M2 operates in saturated mode over the entire target temperature range and the I_{REF} current source is not affected (i.e. the I_{REF} transistor always remains saturated). In detail, this means that the gate voltage is always above $V_{gate,min}$ (M2) and below $V_{gate,max}$ (I_{REF} transistor). At M1, saturation is inherently ensured by the Gate-Drain connection. The same applies to M5/M6 and M7/M8. Saturated operation should be ensured for all of them.

[0079] A small error may result in case a current flow through the transistors M3 and M4 differs and due to the exponential characteristic of the ON resistance (see Fig. 6).

[0080] At the target transistor M4 the bias current/voltage is approximately 0 and the ON resistance in effect acts only dynamically. An improved operation may be possible by separating the transistors M3 and M4 into multiple serially connected MOSFET transistors of equal size, such that the output voltage V_R is equally distributed across the serially connected MOSFET transistors.

[0081] Referring now to Fig. 4, in another embodiment of a circuit arrangement 142 the MOSFET transistor M3 is not connected directly to ground, but in addition a voltage source V1 is arranged in the path between the source S of the MOSFET transistor M3 towards ground. In this way a voltage shift by the voltage V1 may be obtained.

[0082] Other than that, the circuit arrangement 142 of Fig. 4 is functionally identical to the circuit arrangement 140 of Fig. 2.

[0083] Referring now to Fig. 5, in an embodiment of a circuit arrangement 143 to implement a voltage shift as illustrated in Fig. 4, for example a MOSFET transistor M9 may be connected in between the source S of the MOSFET transistor M3 and ground, as illustrated in Fig. 5. In addition, a MOSFET transistor M10 may be connected in between the source S of the MOSFET transistor M4 and ground. The voltage V2 across the MOSFET transistor M9 may be set equal to the voltage V1 between the source S of the MOSFET transistor M4 and ground by suitably designing the drain current of the MOSFET transistor M10 and the channel width and channel length of the MOSFET transistor M9.

[0084] Other than the arrangement of transistors M9, M10, the circuit arrangement 143 of Fig. 5 is functionally identical to the circuit arrangement 140 of Fig. 2.

[0085] The MOSFET transistors M1, M2 in the circuit arrangement 140 of Fig. 2 and likewise in the circuit arrangement 142 of Fig. 4 and the circuit arrangement 143 of Fig. 5 may also be implemented by bipolar transistors.

[0086] The reference current I_{REF} may generally lie in a range between 10 nA and 100 nA, for example at around 20 nA.

[0087] The output voltage V_R may generally lie in a range between 35 mV to 60 mV.

[0088] The ON resistance of the MOSFET transistor M3 may for example have a resistance value in between 500 kOhm to 6 MOhm, wherein the ON resistance of the MOSFET transistor M4 may have a scaling factor from 1 to 100 compared to the resistance of M3, which is resistance value in between 500 kOhm to 600 MOhm.

[0089] The idea underlying the invention is not limited to the embodiments described above, but may be implemented in an entirely different fashion.

[0090] The implantable medical device may be for example an ICD or a CRT-D device or another pacemaker device.

[0091] The implantable medical device may comprise electrode leads carrying electrode poles, which may be implanted to reach into the patient's heart, or may rest fully outside of the patient's heart when they are implanted in the patient. In other embodiments, the implantable medical device is a leadless device not comprising electrode leads.

List of reference numerals

[0092]

1	Implantable medical device
10	Generator
11	Electrode lead
12	Electrode lead
5 13	Electrode lead
14	Processing circuitry
140-144	Circuit arrangement /circuit portion
2	External device
3	Remote server device
10 4	Public communication network
D	Drain of MOSFET transistor
G	Gate of MOSFET transistor
$I_{D, M10}$	Drain current through transistor M10
I_{REF}	Reference current
15 LR	Linear region
M1-M12	MOSFET transistor
MI	Moderate inversion region
P	Patient
R_{REF}	Non-temperature-dependent resistance
20 S	Source of MOSFET transistor
SI	Strong inversion region
V1, V2	Voltage
VCC	Supply voltage
V_{Gate}	Gate voltage
25 V_R	Output voltage
V_{REF}	Reference voltage
WI	Weak inversion region
X, Y	Factor

30 Claims

1. Circuit arrangement (140-144) for use in an implantable medical device (1), configured for providing a temperature-compensated output resistance, comprising:
 - 35 a first MOSFET transistor (M3),
a first circuit portion configured to supply a temperature-dependent reference current (I_{REF}) to the first MOSFET transistor (M3), and
a second circuit portion configured to generate a temperature-dependent output voltage (V_R) across a drain (D) and a source (S) of the first MOSFET transistor (M3), such that an ON resistance ($R_{ON, M3}$) of the first MOSFET transistor (M3) resulting from the output voltage (V_R) and the reference current (I_{REF}) provides the temperature-compensated output resistance.
2. Circuit arrangement (140-144) according to claim 1, wherein the first MOSFET transistor (M3) is configured to operate in a linear region of MOSFET operation.
3. Circuit arrangement (140-144) according to claim 1 or 2, wherein the temperature-dependent reference current (I_{REF}) comprises a first temperature dependency and the temperature-dependent output voltage (V_R) comprises a second temperature dependency, wherein the first temperature dependency and the second temperature dependency are at least approximately equal.
4. Circuit arrangement (140-144) according to one of the preceding claims, wherein the second circuit portion comprises a pair of second MOSFET transistors (M1, M2), wherein gates (G) of the second MOSFET transistors (M1, M2) are connected to each other.
5. Circuit arrangement (140-144) according to claim 4, wherein the second MOSFET transistors (M1, M2) are configured to operate in a weak inversion region of MOSFET operation.
6. Circuit arrangement (140-144) according to claim 4 or 5, wherein the first circuit portion is connected to drains (D) of

the second MOSFET transistors (M1, M2) to supply the reference current (I_{REF}) to the drains (D) of the second MOSFET transistors (M1, M2).

7. Circuit arrangement (140-144) according to one of claims 4 to 6, wherein the drain (D) of one of the second MOSFET transistors (M1, M2) is connected to a gate (G) of the first MOSFET transistor (M3).
8. Circuit arrangement (140-144) according to claim 7, wherein the source (S) of said one of the second MOSFET transistors (M1, M2) is connected to the drain (D) of the first MOSFET transistor (M3).
9. Circuit arrangement (140-144) according to one of claims 4 to 8, wherein the drain (D) and the gate (G) of the other of the second MOSFET transistors (M1, M2) are connected to each other.
10. Circuit arrangement (140-144) according to one of the preceding claims, wherein the first circuit portion comprises a pair of third MOSFET transistors (M5, M6), wherein gates (G) of the third MOSFET transistors (M5, M6) are connected to each other.
11. Circuit arrangement (140-144) according to claim 10, wherein the third MOSFET transistors (M5, M6) are configured to operate in a weak inversion region of MOSFET operation.
12. Circuit arrangement (140-144) according to claim 10 or 11, wherein the first circuit portion comprises a pair of fourth MOSFET transistors (M7, M8) connected at their gates (G) and serving as a current mirror, wherein a drain (D) of each of the fourth p-type MOSFET transistors (M7, M8) is connected to a drain (D) of one of the third MOSFET transistors (M5, M6).
13. Circuit arrangement (140-144) according to one of claims 10 to 12, wherein one of the third MOSFET transistors (M5, M6) at its source (S) is connected to a non-temperature-dependent resistance (R_{REF}), wherein the first circuit portion is configured to output said reference current (I_{REF}) according to a reference voltage (V_{REF}) produced across said non-temperature-dependent resistance (R_{REF}).
14. Circuit arrangement (140-144) according to one of the preceding claims, wherein the gate (G) of the first MOSFET transistor (M3) is connected to a gate (G) of a target transistor (M4) to produce a temperature-independent ON resistance at the target transistor (M4).
15. Implantable medical device (1) for performing a therapeutic and/or diagnostic function in a patient (P), comprising a circuit arrangement (140-144) according to one of the preceding claims.

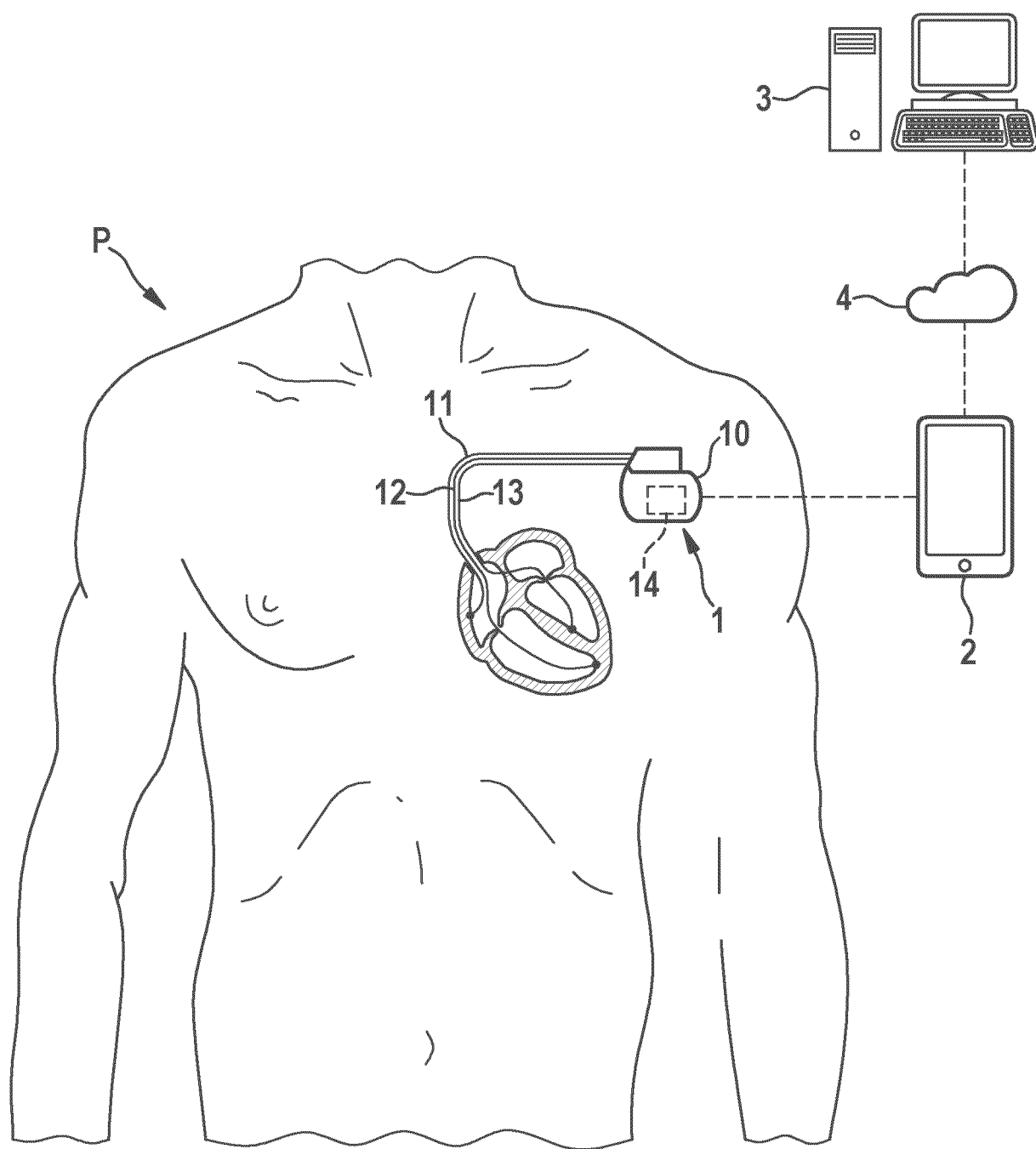


Fig. 1

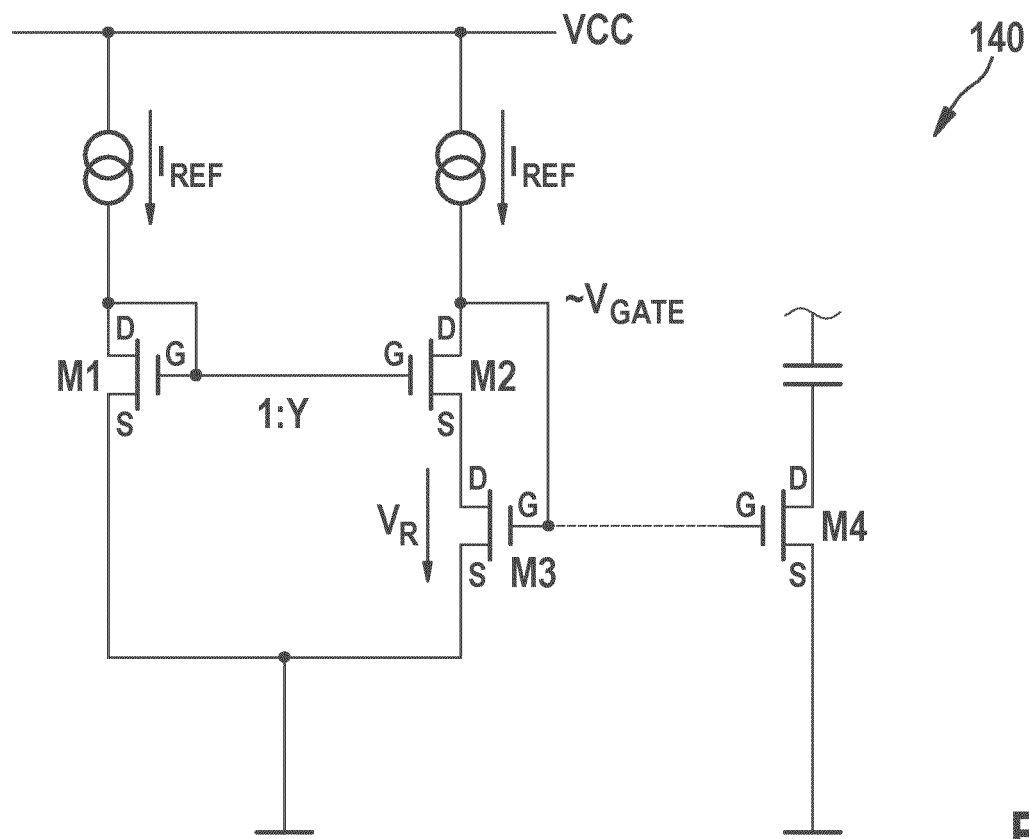


FIG. 2

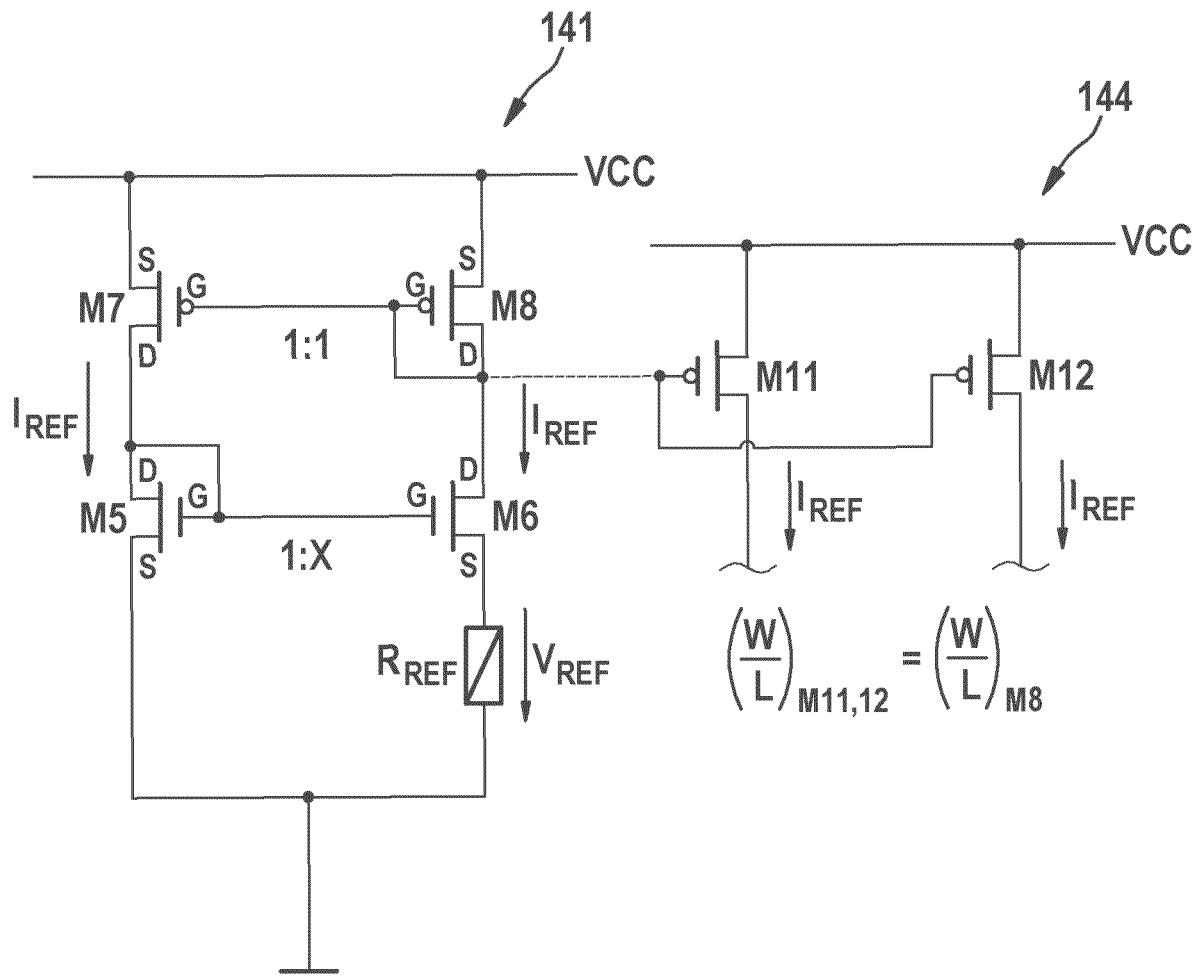
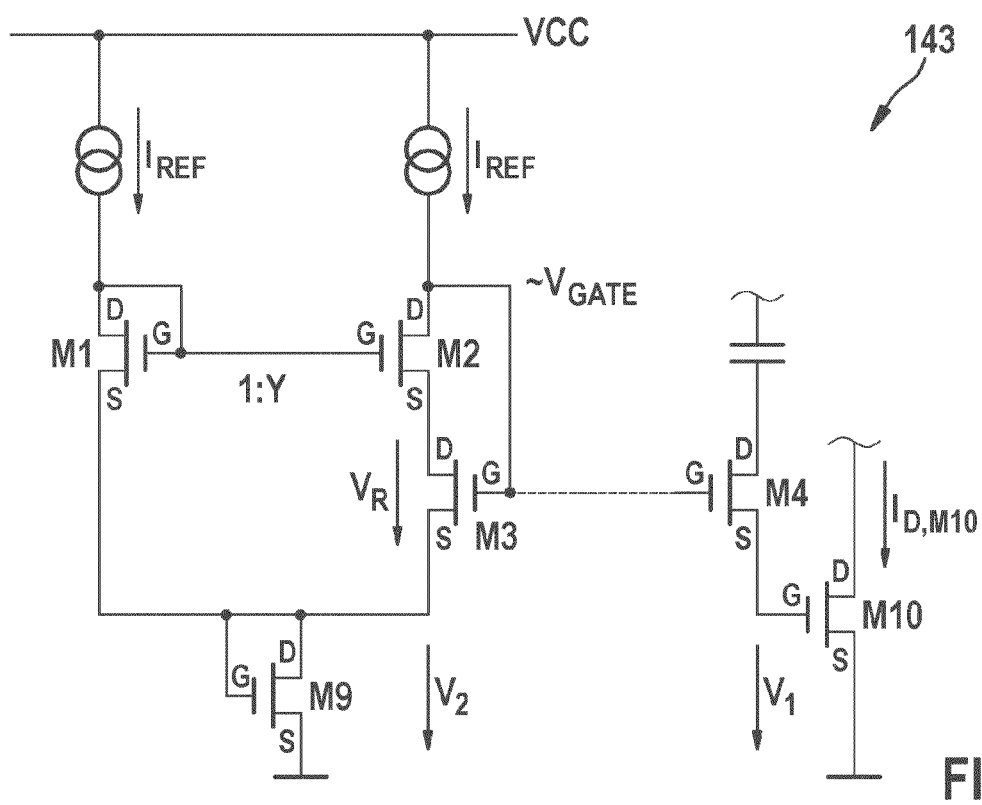
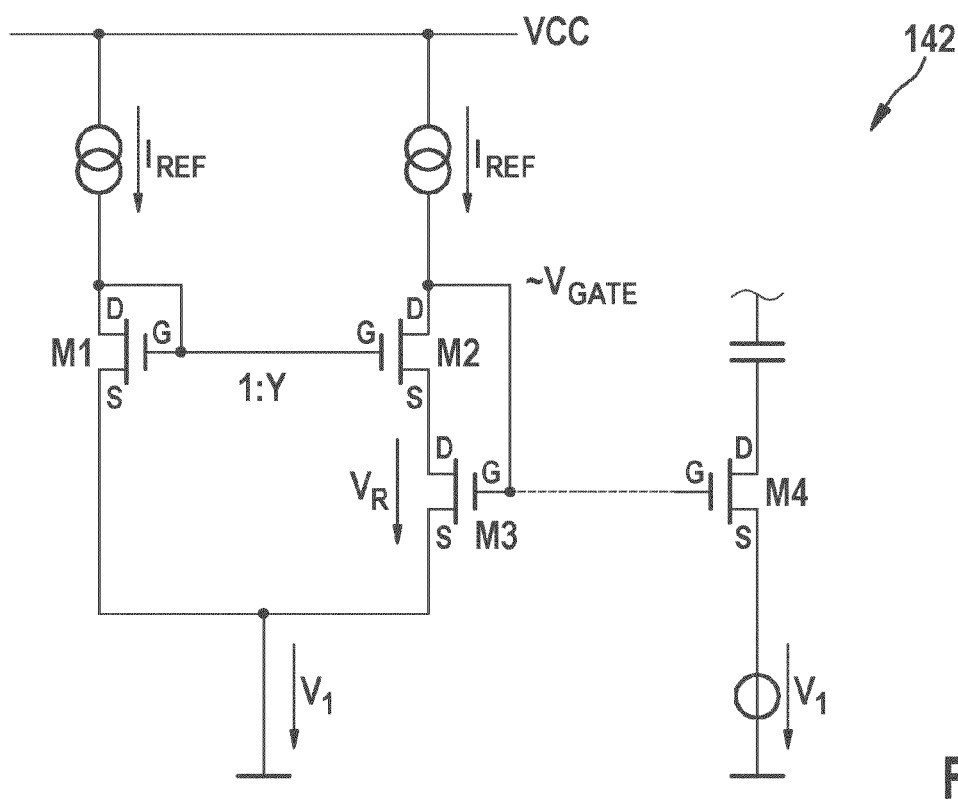


FIG. 3



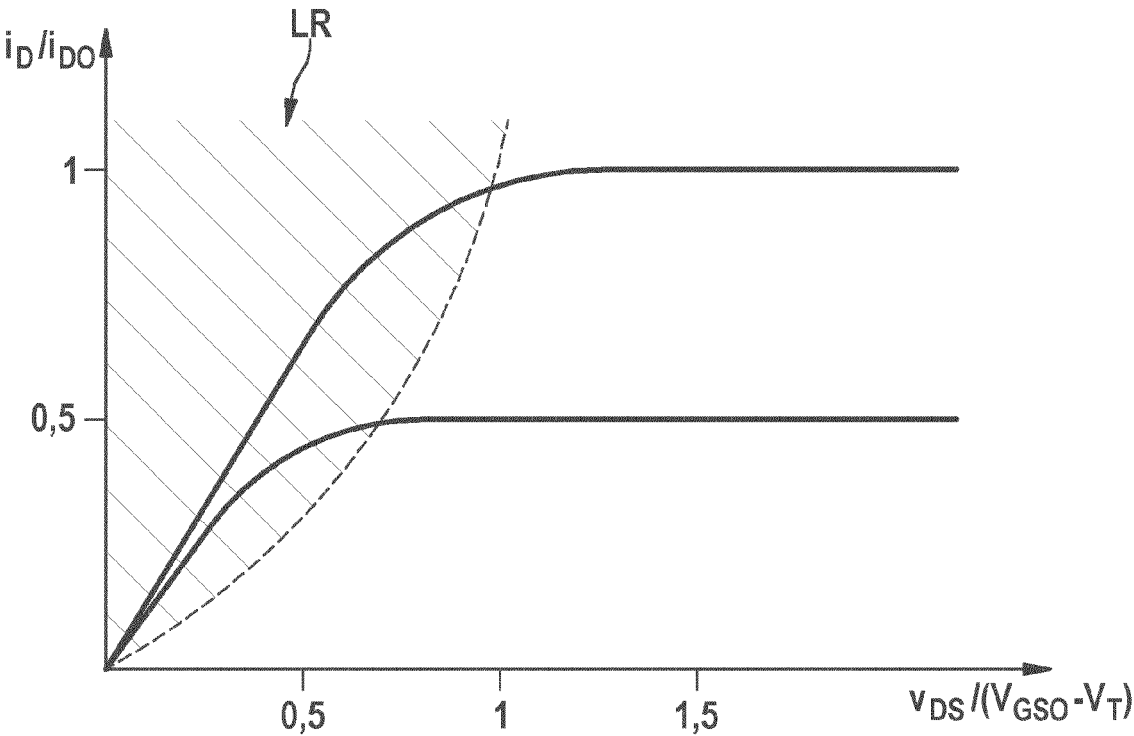


FIG. 6

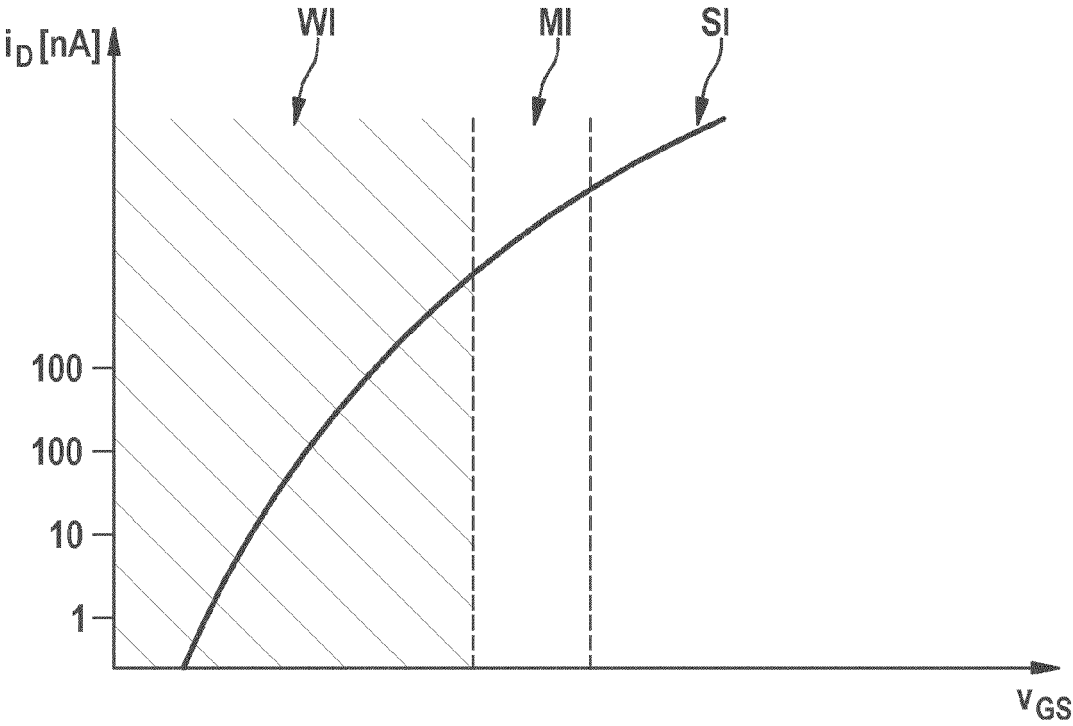


FIG. 7



EUROPEAN SEARCH REPORT

Application Number

EP 24 18 8848

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	ZHANG TAN-TAN ET AL: "A BJT-Based Temperature Sensor in 40-nm CMOS With 0.8°C(3[sigma]) Untrimmed Inaccuracy", 2019 32ND IEEE INTERNATIONAL SYSTEM-ON-CHIP CONFERENCE (SOCC), IEEE, 3 September 2019 (2019-09-03), pages 1-4, XP033768815, DOI: 10.1109/SOCC46988.2019.1570555725 [retrieved on 2020-05-05] * abstract; figures 2,3 *	1-3,15	INV. G05F3/24 G05F3/30
X	EP 3 210 215 B1 (MURATA MANUFACTURING CO [JP]; MASSACHUSETTS INST TECHNOLOGY [US]) 6 March 2024 (2024-03-06) * abstract; figures 1,2 *	1-15	
X	US 2012/274306 A1 (MARINCA STEFAN [IE]) 1 November 2012 (2012-11-01) * abstract; figure 3a *	1,2,4-9, 15	
			TECHNICAL FIELDS SEARCHED (IPC)
			G05F
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
The Hague		20 December 2024	Arias Pérez, Jagoba
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			
T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03.82 (P34C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 24 18 8848

5

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

20-12-2024

10

15

20

25

30

35

40

45

50

55

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
EP 3210215	B1	06-03-2024	CN	106796833 A	31-05-2017
			EP	3210215 A1	30-08-2017
			JP	6328849 B2	23-05-2018
			JP	2017534171 A	16-11-2017
			US	2018115303 A1	26-04-2018
			WO	2016064380 A1	28-04-2016

US 2012274306	A1	01-11-2012	CN	102369495 A	07-03-2012
			EP	2414905 A1	08-02-2012
			JP	5710586 B2	30-04-2015
			JP	2012522313 A	20-09-2012
			US	2010244808 A1	30-09-2010
			US	2012274306 A1	01-11-2012
			WO	2010114720 A1	07-10-2010

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Non-patent literature cited in the description

- **PHILLIP E. ALLEN ; DOUGLAS R. HOLBERG.**
CMOS analog circuit design, 1987, ISBN
0-19-510720-9 [0016] [0022] [0054]