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(54) METHOD FOR REFRESHING DISPLAY IN PARTITIONED MANNER, DISPLAY SYSTEM, AND ELECTRONIC DEVICE

(57) A partition refresh method of a display (10), a display system (60), and an electronic device (100) are provided. More enable signal lines are introduced to the display (10), to provide an enable signal for cascaded GOA units (220) for a longer time, thereby providing a condition for increasing a pulse width of a data holding signal output by the GOA unit (220) and creating a non-coupling area. In addition, in the partition refresh method of the display (10), the pulse width of the data holding signal output by the GOA unit (220) is increased, and a data writing control signal is controlled to appear after a coupling area, so that data writing into a pixel unit (210) is not interfered by a glitch of the data holding signal, to avoid a screen horizontal stripe.

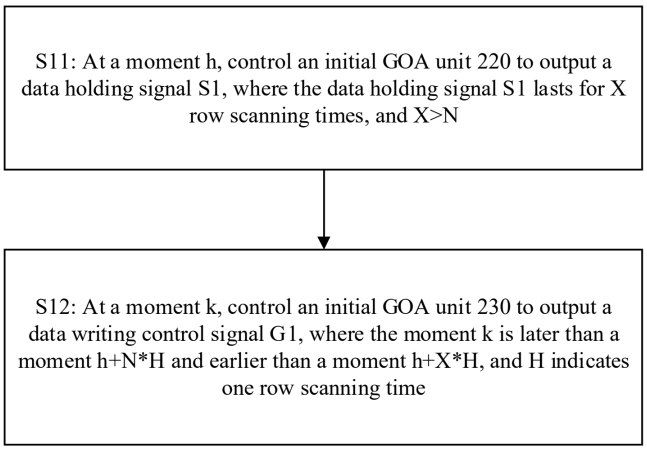

FIG. 7

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Description

[0001] This application claims priority to Chinese Patent Application No. 202311554390.2, filed with the China National Intellectual Property Administration on November 17, 2023, and entitled "PARTITION REFRESH METHOD OF DISPLAY, DISPLAY SYSTEM, AND ELECTRONIC DEVICE", which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] This application relates to the field of electronic technologies, and in particular, to a partition refresh method of a display, a display system, and an electronic device.

BACKGROUND

[0003] With development of display technologies, to ensure smooth display of a picture, screen refresh rates supported by electronic devices such as mobile phones and tablet computers are continuously increased. However, power consumption of displays poses a great challenge to power saving or battery lives of the devices. To address this, displays that support a low refresh rate or even an ultra-low refresh rate are gradually introduced to the market in recent years, for example, low-temperature polycrystalline oxide (low-temperature polycrystalline oxide, LTPO) displays that support a refresh rate down to 1 Hz. Nevertheless, a current refresh manner of a display component is full-screen refresh. When only a small part of a picture on a screen needs to be updated, a display driver integrated circuit (display driver integrated circuit, DDIC) still refreshes the entire picture on the screen, resulting in unnecessary power consumption.

SUMMARY

[0004] Embodiments of this application provide a partition refresh method of a display and an electronic device, to resolve one or more problems such as a screen horizontal stripe, a luminance difference between a low refresh area and a high refresh area, and screen flickering while a partition variable frequency function is supported.

[0005] According to a first aspect, an embodiment of this application provides a partition refresh method of a display. The method may be applied to the display. The display may include a display circuit, a first gate on array GOA circuit, and a second GOA circuit, a display panel includes a plurality of pixel units, the first GOA circuit includes M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit includes cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2.

[0006] The method may include:

at a moment h, controlling an initial first GOA unit to output the data holding signal, where the data holding signal lasts for X row scanning times, and X>N; and

at a moment k, controlling an initial second GOA unit to output the data writing control signal, where the moment k is later than a moment h+N*H and earlier than a moment h+X*H, and H indicates one row scanning time.

[0007] In the first aspect, the display may be the display 10 mentioned in subsequent embodiments, the display circuit, the first GOA circuit, and the second GOA circuit may be the display circuit 21, the GOA circuit 22, and the GOA circuit 23 mentioned in subsequent embodiments, and the first GOA unit and the second GOA unit may be the GOA unit 220 and the GOA unit 230 mentioned in subsequent embodiments.

[0008] According to the method provided in the first aspect, more enable signal lines are introduced to the display 10, so that enable signals may be provided for cascaded GOA units 220 for a longer time, to provide a condition for increasing a pulse width of a data holding signal S1 and creating a non-coupling area. In addition, a pulse width of the data holding signal S1 is at least greater than N row scanning times, to ensure that a pulse width of a data holding signal S1 output by each GOA unit 220 includes a non-coupling area. In addition, the moment k is later than the moment h+N*H, so that a data writing control signal G1 may appear after a coupling area of the data holding signal S1, so that data writing into the pixel unit is not affected by a glitch of S1, and no screen horizontal stripe appears.

[0009] With reference to the first aspect, in some embodiments, controlling the initial first GOA unit to output the data holding signal may specifically include: controlling an i^{th} first GOA unit in the cascaded M*N first GOA units to output the data holding signal at a moment h+(i-1)*Q*H, where i is a positive integer, i≤M*N, Q indicates that the data holding signal S1 output by the i^{th} GOA unit 220 is Q row scanning times earlier than a data holding signal S1 output by an $(i+1)^{th}$ GOA unit 220, and a value of Q may be a positive integer, for example, 1 or 2.

[0010] With reference to the first aspect, in some embodiments, controlling the initial first GOA unit to output the data holding signal may specifically include: inputting a start vertical STV signal to an input end of the initial first GOA unit at a moment h-Q*H, where Q indicates that the i^{th} first GOA unit outputs the data holding signal Q row scanning times earlier than the $(i+1)^{th}$ first GOA unit.

[0011] With reference to the first aspect, in some embodiments, a calculation formula for a maximum value X_{max} of X may be as follows: X_{max}=M*Y-(M*N-1)*Q, Y

indicates a pulse width of an enable signal on an enable signal line, and Q indicates that the i^{th} first GOA unit outputs the data holding signal Q row scanning times earlier than the $(i+1)^{th}$ first GOA unit. It can be learned that greater M indicates greater X_{max}, that is, increasing a quantity of VFE signals can increase the pulse width of the signal S1.

[0012] With reference to the first aspect, in some embodiments, controlling the initial second GOA unit to output the data writing control signal may specifically include: a j^{th} second GOA unit in the cascaded second GOA units starts to output the data writing control signal at a moment k+(j-1)*q, where q indicates a time by which the j^{th} second GOA unit outputs the data writing control signal later than a $(j-1)^{th}$ second GOA unit, j is a positive integer, and j is less than or equal to a quantity of the cascaded second GOA units.

[0013] With reference to the first aspect, in some embodiments, controlling the initial second GOA unit to output the data writing control signal may specifically include: inputting a start vertical STV signal to an input end of the initial second GOA unit at a moment k-q, where q indicates the time by which the j^{th} second GOA unit outputs the data writing control signal later than the $(j-1)^{th}$ second GOA unit.

[0014] With reference to the first aspect, in some embodiments, the VFE signal may be a high-level signal, and the data holding signal may also be a high-level signal. The method provided in the first aspect may further include: controlling a time at which the enable signal on the enable signal line switches from a high level to a low level to be later than a first time, where the first time is a time at which the data holding signal output by a last first GOA unit connected to the enable signal line switches from a high level to a low level.

[0015] According to a second aspect, an embodiment of this application provides a partition refresh method of a display. The method may be applied to the display. The display may include a display circuit, a first gate on array GOA circuit, and a second GOA circuit, a display panel includes a plurality of pixel units, the first GOA circuit includes M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit includes cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2.

[0016] The method may include:

determining a time for performing data writing into a pixel unit in a first screen area; and

when performing data writing into the pixel unit in the first screen area, performing first bias processing on a reset voltage of the pixel unit in the first screen area, where a reset voltage after the first bias processing is a reset voltage corresponding to a first reference luminance at a first refresh rate during data writing; and

the first reference luminance is less than a luminance corresponding to the reset voltage of the pixel unit in the first screen area at the first refresh rate before the first bias processing.

[0017] In the second aspect, the display may be the display 10 mentioned in subsequent embodiments, the display circuit, the first GOA circuit, and the second GOA circuit may be the display circuit 21, the GOA circuit 22, and the GOA circuit 23 mentioned in subsequent embodiments, and the first GOA unit and the second GOA unit may be the GOA unit 220 and the GOA unit 230 mentioned in subsequent embodiments.

[0018] According to the method provided in the second aspect, the reset voltage Vref of the pixel unit is adjusted, so that a luminance of the first screen area with a low refresh rate during data writing may be adjusted to the first reference luminance, and a luminance difference between different screen partitions can be reduced.

[0019] With reference to the second aspect, in some embodiments, the first reference luminance may be specifically a luminance corresponding to a first reset voltage at a second refresh rate during data writing, the first reset voltage is a reset voltage of a pixel unit in a second screen area during data writing into the second screen area under refresh at the second refresh rate, and the second refresh rate is higher than the first refresh rate.

[0020] The first reference luminance may be specifically a luminance corresponding to a first reset voltage at a second refresh rate during data writing, and the first reset voltage is a reset voltage of a pixel unit in a second screen area during data writing into the second screen area under refresh at the second refresh rate, and may be measured by a DDIC. The first refresh rate is lower than the second refresh rate. In this way, the luminance of the first screen area with the low refresh rate may be adjusted to a luminance of the second screen area with a high refresh rate, to unify luminances of partitions with different refresh rates and reduce a luminance difference.

[0021] With reference to the second aspect, in some embodiments, a luminance and a reset voltage Vref during data writing have different correspondences at different refresh rates. In addition, the correspondence may be further measured and recorded in advance, to adjust the reset voltage during data writing, and unify screen luminances. A first mapping table may be used to record a correspondence between a reset voltage and a luminance during data writing at the second refresh rate, and a second mapping table may be used to record a correspondence between a reset voltage and a luminance during data writing at the first refresh rate.

[0022] The method provided in the second aspect may further include: searching the first mapping table for a luminance corresponding to the first reset voltage, and determining the found luminance as the first reference

luminance; and searching the second mapping table for a reset voltage corresponding to the first reference luminance, and determining the found reset voltage as the reset voltage after the first bias processing.

[0023] According to a third aspect, an embodiment of this application provides a partition refresh method of a display. The method may be applied to the display. The display may include a display circuit, a first gate on array GOA circuit, and a second GOA circuit, a display panel includes a plurality of pixel units, the first GOA circuit includes M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit includes cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2.

[0024] The method may include:

determining a time for skipping performing data writing into a pixel unit in a third screen area, where a refresh rate of the third screen area is a third refresh rate; and

when skipping performing data writing into the pixel unit in the third screen area, performing second bias processing on a reset voltage of the pixel unit in the third screen area, where a reset voltage after the second bias processing is a reset voltage corresponding to a second reference luminance at the third refresh rate during data holding; and

the second reference luminance is a luminance corresponding to a second reset voltage at the third refresh rate during data writing, and the second reset voltage is a reset voltage during data writing into the third screen area at the third refresh rate.

[0025] In the third aspect, the display may be the display 10 mentioned in subsequent embodiments, the display circuit, the first GOA circuit, and the second GOA circuit may be the display circuit 21, the GOA circuit 22, and the GOA circuit 23 mentioned in subsequent embodiments, and the first GOA unit and the second GOA unit may be the GOA unit 220 and the GOA unit 230 mentioned in subsequent embodiments.

[0026] According to the method provided in the third aspect, the reset voltage Vref of the pixel unit is adjusted, so that a luminance of the screen area during data holding may be adjusted to a luminance of the screen area during data writing, and the luminance of the screen area may be kept without sudden changes during switching between data holding and data writing, to avoid screen flickering.

[0027] With reference to the third aspect, in some embodiments, the second reset voltage is a reset voltage during data writing into the third screen area at the third refresh rate, and may be measured by a DDIC. The method provided in the third aspect may further include: obtaining the second reset voltage through measurement.

[0028] With reference to the third aspect, in some embodiments, the method provided in the third aspect may further include: determining a time for performing data writing into the pixel unit in the third screen area.

[0029] With reference to the third aspect, in some embodiments, correspondences between luminances and reset voltages Vref at different refresh rates may be measured and recorded in advance, to adjust a reset voltage during data holding. Based on the correspondence, a luminance value corresponding to a reset voltage at a specific refresh rate during data writing may be determined, and a reset voltage corresponding to a luminance at a specific refresh rate during data writing may also be determined. A third mapping table is used to record a correspondence between a reset voltage and a luminance during data writing at the third refresh rate, and a fourth mapping table is used to record a correspondence between a reset voltage and a luminance during data holding at the third refresh rate.

[0030] The method provided in the third aspect may further include: searching the third mapping table for a luminance corresponding to the second reset voltage, and determining the found luminance as the second reference luminance; and searching the fourth mapping table for a reset voltage corresponding to the second reference luminance, and determining the found reset voltage as the reset voltage after the second bias processing.

[0031] With reference to the third aspect, in some embodiments, the third screen area may be a low-refresh-rate screen area, for example, the foregoing first screen area. In this case, the third refresh rate is a low refresh rate and may be the same as the foregoing first refresh rate, and the third mapping table may be the same as the foregoing second mapping table. The third screen area may alternatively be a high-refresh-rate screen area, for example, the foregoing second screen area. In this case, the third refresh rate is a high refresh rate and may be the same as the foregoing second refresh rate, and the fourth mapping table may be the same as the foregoing first mapping table.

[0032] With reference to the third aspect, in some embodiments, when the third screen area is a low-refresh-rate screen area, the second reset voltage may further be the reset voltage after the first bias processing in the method provided in the second aspect.

[0033] The method provided in the third aspect may further include: before performing the second bias processing, determining a time for writing data into a pixel unit in the first screen area; and when performing data writing into the pixel unit in the first screen area, performing first bias processing on a reset voltage of the pixel unit in the first screen area, where a reset voltage after the first bias processing is a reset voltage corresponding to a first reference luminance at the first refresh rate during data

writing; and the first reference luminance is specifically a luminance corresponding to a first reset voltage at a second refresh rate during data writing, the first reset voltage is a reset voltage of a pixel unit in a second screen area during data writing into the second screen area under refresh at the second refresh rate, and the second refresh rate is higher than the first refresh rate.

[0034] With reference to the third aspect, in some embodiments, the first reset voltage is the reset voltage of the pixel unit in the second screen area during data writing into the second screen area under refresh at the second refresh rate, and may be measured by the DDIC. The method provided in the third aspect may further include: obtaining the first reset voltage through measurement.

[0035] With reference to the third aspect, in some embodiments, the second screen area may be a screen area with a highest refresh rate.

[0036] With reference to the third aspect, in some embodiments, a first mapping table may be used to record a correspondence between a reset voltage and a luminance during data writing at the second refresh rate, and a second mapping table may be used to record a correspondence between a reset voltage and a luminance during data writing at the first refresh rate.

[0037] The method provided in the third aspect may further include: searching the first mapping table for a luminance corresponding to the first reset voltage, and determining the found luminance as the first reference luminance; and searching the second mapping table for a reset voltage corresponding to the first reference luminance, and determining the found reset voltage as the reset voltage after the first bias processing.

[0038] According to a fourth aspect, an embodiment of this application provides a partition refresh method of a display. The method may be applied to the display. The display may include a display circuit, a first gate on array GOA circuit, and a second GOA circuit, a display panel includes a plurality of pixel units, the first GOA circuit includes M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit includes cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2.

[0039] The method may include:

determining a gray scale of a pixel unit in a first screen area; and

when performing data writing into a first pixel unit in the first screen area, performing third bias processing on a data voltage of the first pixel unit, where a data voltage after the third bias processing is a data voltage corresponding to a third reference luminance at a first refresh rate during data writing, and the first pixel unit is a pixel unit whose gray scale is a first gray scale in the first screen area; and

the third reference luminance is a luminance corresponding to a first data voltage at a second refresh rate, the first data voltage is a data voltage during data writing into a second pixel unit at the second refresh rate, the second pixel unit is a pixel unit whose gray scale is the first gray scale in a second screen area, a refresh rate of the second screen area is the second refresh rate, and the second refresh rate is greater than the first refresh rate.

[0040] In the fourth aspect, the display may be the display 10 mentioned in subsequent embodiments, the display circuit, the first GOA circuit, and the second GOA circuit may be the display circuit 21, the GOA circuit 22, and the GOA circuit 23 mentioned in subsequent embodiments, and the first GOA unit and the second GOA unit may be the GOA unit 220 and the GOA unit 230 mentioned in subsequent embodiments.

[0041] According to the method provided in the fourth aspect, adjusting a data voltage Vdata of a pixel unit can reduce a luminance difference between a high-refresh-rate area and a low-refresh-rate area at a same gray scale.

[0042] With reference to the fourth aspect, in some embodiments, the method may further include: obtaining the first data voltage through measurement.

[0043] With reference to the fourth aspect, in some embodiments, correspondences between luminances and data voltages Vdata at different refresh rates during data writing may be measured and recorded in advance, to adjust the data voltage Vdata. Based on the correspondence, a luminance value corresponding to a data voltage Vdata at a specific refresh rate may be determined, and a data voltage Vdata corresponding to a luminance at a specific refresh rate may also be determined. A fifth mapping table is used to record a correspondence between a data voltage and a luminance during data writing at the second refresh rate, and a sixth mapping table is used to record a correspondence between a data voltage and a luminance during data writing at the first refresh rate.

[0044] The method provided in the fourth aspect may further include:

searching the fifth mapping table for a luminance corresponding to the first data voltage, and determining the found luminance as the third reference luminance; and

searching the sixth mapping table for a data voltage corresponding to the third reference luminance, and determining the found luminance as the data voltage after the third bias processing.

[0045] According to a fifth aspect, an embodiment of this application provides a partition refresh method of a display. The method may be applied to the display. The display may include a display circuit, a first gate on array GOA circuit, and a second GOA circuit, a display panel includes a plurality of pixel units, the first GOA circuit

includes M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit includes cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2.

[0046] The method may include:

determining a time for skipping performing data writing into a pixel unit in a fourth screen area, where a refresh rate of the fourth screen area is a fourth refresh rate; and

when skipping performing data writing into the pixel unit in the fourth screen area, performing fourth bias processing on a data voltage of a third pixel unit in the fourth screen area, where a data voltage after the fourth bias processing is a data voltage corresponding to a fourth reference luminance at the fourth refresh rate during data holding; and

the fourth reference luminance is a luminance corresponding to a second data voltage at the fourth refresh rate during data writing into the fourth screen area, and the second data voltage is a data voltage during data writing into the third pixel unit at the fourth refresh rate.

[0047] In the fifth aspect, the display may be the display 10 mentioned in subsequent embodiments, the display circuit, the first GOA circuit, and the second GOA circuit may be the display circuit 21, the GOA circuit 22, and the GOA circuit 23 mentioned in subsequent embodiments, and the first GOA unit and the second GOA unit may be the GOA unit 220 and the GOA unit 230 mentioned in subsequent embodiments.

[0048] According to the method provided in the fifth aspect, adjusting a data voltage Vdata of a pixel unit can avoid screen flickering.

[0049] With reference to the fifth aspect, in some embodiments, the method may further include: obtaining the second data voltage through measurement.

[0050] With reference to the fifth aspect, in some embodiments, the method may further include: determining a time for skipping performing data writing into the fourth screen area.

[0051] With reference to the fifth aspect, in some embodiments, correspondences between luminances and data voltages Vdata at different refresh rates during data holding may be measured and recorded in advance, to adjust the data voltage during data holding. Based on the correspondence, a luminance value corresponding to a data voltage at a specific refresh rate during data holding may be determined, and a data voltage corresponding to a luminance at a specific refresh rate during data holding may also be determined. A seventh mapping table is used to record a correspondence between a data voltage and a luminance during data writing at the fourth refresh rate, and an eighth mapping table is used to record a correspondence between a data voltage and a luminance during data holding at the fourth refresh rate.

[0052] The method provided in the fifth aspect may further include: searching the seventh mapping table for a luminance corresponding to the second data voltage, and determining the found luminance as the fourth reference luminance; and searching the eighth mapping table for a data voltage corresponding to the fourth reference luminance, and determining the found data voltage as the data voltage after the fourth bias processing.

[0053] With reference to the fifth aspect, in some embodiments, the fourth screen area may be a low-refresh-rate screen area, for example, the foregoing first screen area. In this case, the fourth refresh rate is a low refresh rate and may be the same as the foregoing first refresh rate, and the seventh mapping table may be the same as the foregoing sixth mapping table. The fourth screen area may alternatively be a high-refresh-rate screen area, for example, the foregoing second screen area. In this case, the fourth refresh rate is a high refresh rate and may be the same as the foregoing second refresh rate, and the eighth mapping table may be the same as the foregoing fifth mapping table.

[0054] With reference to the fifth aspect, in some embodiments, if the fourth screen area is specifically the first screen area, and the fourth refresh rate is specifically the first refresh rate, before performing the fourth bias, the method may further include: determining a gray scale of a pixel unit in the first screen area; and when performing data writing into a first pixel unit in the first screen area, performing third bias processing on a data voltage of the first pixel unit, where a data voltage after the third bias processing is a data voltage corresponding to a third reference luminance at the first refresh rate during data writing, and the first pixel unit is a pixel unit whose gray scale is a first gray scale in the first screen area; and the third reference luminance is a luminance corresponding to a first data voltage at a second refresh rate, the first data voltage is a data voltage during data writing into a second pixel unit at the second refresh rate, the second pixel unit is a pixel unit whose gray scale is the first gray scale in a second screen area, a refresh rate of the second screen area is the second refresh rate, and the second refresh rate is greater than the first refresh rate.

[0055] With reference to the fifth aspect, in some embodiments, the method may further include: obtaining the first data voltage through measurement.

[0056] With reference to the fifth aspect, in some embodiments, the method may further include: searching a fifth mapping table for a luminance corresponding to the first data voltage, and determining the found luminance as the third reference luminance; and searching a sixth mapping table for a data voltage corresponding to the third reference luminance, and determining the found luminance as the data voltage after the third bias processing, where the fifth mapping table is used to record a

correspondence between a data voltage and a luminance during data writing at the second refresh rate, and the sixth mapping table is used to record a correspondence between a data voltage and a luminance during data writing at the first refresh rate.

[0057] According to a sixth aspect, an embodiment of this application provides an electronic device. The electronic device may include a display, a processor, and a memory. The display is coupled to the processor, and the memory is coupled to the processor.

[0058] The display includes a display panel, a first gate on array GOA circuit, and a second GOA circuit, the display panel includes a plurality of pixel units, the first GOA circuit includes M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit includes cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2.

[0059] The memory is configured to store computer program code. The computer program code includes computer instructions. When the processor executes the computer instructions, the electronic device is enabled to perform the method described in any one or more of embodiments of the first aspect, the second aspect, the third aspect, the fourth aspect, or the fifth aspect.

[0060] According to a seventh aspect, an embodiment of this application provides a display system. The display system may include a display and a control circuit.

[0061] The display includes a display panel, a first gate on array GOA circuit, and a second GOA circuit, the display panel includes a plurality of pixel units, the first GOA circuit includes M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit includes cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2. The control circuit is configured to invoke computer instructions, so that the display system can perform the method described in any one or more of embodiments of the first aspect, the second aspect, the third aspect, the fourth aspect, or the fifth aspect.

[0062] According to an eighth aspect, an embodiment of this application provides a chip system. The chip system is used in an electronic device. The chip system includes one or more processors. The processor is configured to invoke computer instructions, so that the electronic device can perform the method described in any one or more of embodiments of the first aspect, the second aspect, the third aspect, the fourth aspect, or the fifth aspect.

[0063] According to a ninth aspect, this application provides a computer-readable storage medium, including a computer executable program. When the computer executable program is run on an electronic device, the electronic device is enabled to perform the method described in any one or more of embodiments of the first aspect, the second aspect, the third aspect, the fourth aspect, or the fifth aspect.

[0064] According to a tenth aspect, this application provides a computer program product including instructions. When the computer program product is run on an electronic device, the electronic device is enabled to perform the method described in any one or more of embodiments of the first aspect, the second aspect, the third aspect, the fourth aspect, or the fifth aspect.

BRIEF DESCRIPTION OF DRAWINGS

[0065] To describe the technical solutions in embodiments of this application or in the background more clearly, the following describes the accompanying drawings for describing embodiments of this application or the background.

FIG. 1 shows a display 10 according to an embodiment of this application;

FIG. 2 shows an example of a screen area of partition variable frequency display;

FIG. 3 shows a basic structure of an LPTO pixel unit;

FIG. 4 briefly shows timing logic of an output signal and an input signal of each component of the display 10;

FIG. 5 shows screen horizontal stripes generated by a display with a partition variable frequency function;

FIG. 6 shows signal timing present when a display uses two VFE signal lines;

FIG. 7 shows an overall procedure of a partition refresh method of a display according to an embodiment of this application;

FIG. 8 shows signal timing generated in the method shown in FIG. 7;

FIG. 9 shows a screen dark line generated by a display with a partition variable frequency function;

FIG. 10 shows a problem of a luminance difference between screen partitions of a display with a partition variable frequency function;

FIG. 11 shows a luminance difference between a writing frame and a holding frame at a refresh rate of 1 Hz;

FIG. 12 shows an overall procedure of another partition refresh method of a display according to an embodiment of this application;

FIG. 13 shows correspondences between luminances and reset voltages during data writing at refresh rates of 1 Hz and 120 Hz;

FIG. 14 shows an overall procedure of another partition refresh method of a display according to an

embodiment of this application;

FIG. 15 shows correspondences between luminances and reset voltages during data holding at refresh rates of 1 Hz and 120 Hz;

FIG. 16 shows a voltage bias of a reset voltage of a low-refresh-rate area relative to a reset voltage of a high-refresh-rate area during data writing, and a voltage bias of a reset voltage during data holding relative to a reset voltage during data writing;

FIG. 17 shows an overall procedure of another partition refresh method of a display according to an embodiment of this application;

FIG. 18 shows correspondences between luminances and data voltages during data writing at refresh rates of 1 Hz and 120 Hz;

FIG. 19 shows a voltage bias of a data voltage of a low-refresh-rate area relative to a data voltage of a high-refresh-rate area during data writing for implementing a same gray scale;

FIG. 20 shows an overall procedure of another partition refresh method of a display according to an embodiment of this application;

FIG. 21 shows correspondences between luminances and data voltages during data holding at refresh rates of 1 Hz and 120 Hz;

FIG. 22 shows a voltage bias of a data voltage of a low-refresh-rate area relative to a data voltage of a high-refresh-rate area during data writing and a voltage bias of a data voltage during data holding relative to a data voltage during data writing for implementing a same gray scale;

FIG. 23 shows a display system according to an embodiment of this application; and

FIG. 24 shows an electronic device according to an embodiment of this application.

DESCRIPTION OF EMBODIMENTS

[0066] Terms used in the following embodiments of this application are merely intended to describe specific embodiments, but are not intended to limit this application.

[0067] The terms "one", "a", "the", "the foregoing", "this", and "the one" of singular forms used in this specification and the appended claims of this application are also intended to include plural forms, unless otherwise specified in the context clearly. It should also be understood that the term "and/or" used in this application means and includes any or all possible combinations of one or more listed items.

[0068] FIG. 1 shows a display 10 according to an embodiment of this application.

[0069] The display 10 has a partition variable frequency function, that is, different refresh rates may be used in different areas of a screen, to ensure a high refresh rate and power consumption reduction. When a picture of a screen area needs to be updated, a DDIC may perform data writing into the screen area, and for another screen area on which no picture needs to be updated, the DDIC may not perform data writing. This reduces power consumption of a driver chip. For example, as shown in FIG. 2, the screen is divided into three areas, refresh rates of an upper area and a lower area are 120 Hz, and a refresh rate of a middle area is 1 Hz. The middle area is set to a low refresh rate because for a long time, no picture needs to be updated. In this way, the entire screen does not need to use a high refresh rate of 120 Hz. This significantly reduces power consumption of the driver chip.

[0070] The refresh rate is a quantity of times that the display refreshes a displayed picture within one second. For example, a refresh rate of 60 Hz indicates that the display refreshes the displayed picture 60 times within one second.

[0071] To support a partition variable frequency function, the display 10 may use a gate on array (Gate On Array, GOA) technology. GOA can implement a progressive scanning drive function of the display.

[0072] As shown in FIG. 1, the display 10 may include a display circuit 21, a GOA circuit 22, and a GOA circuit 23.

[0073] The display circuit 21 may include M*N*P pixel units 210. M indicates a quantity of enable signals connected to the GOA circuit 22, N indicates a quantity of GOA units 220 connected to one enable signal, and P indicates a quantity of pixel units 210 connected to one GOA unit 220, and also indicates a quantity of pixel rows driven by the GOA unit 220. M, N, and P are positive integers.

[0074] In this embodiment of this application, "*" in each operation expression indicates a multiplication operation. The multiplication operation is not limited to "*", and may also be indicated by "×".

[0075] One pixel unit 210 may be responsible for displaying one row. One pixel unit 210 may have a data holding signal input end (denoted as 2), a data writing control signal input end (denoted as 1), a data signal input end (denoted as Data), and one or more reset voltage input ends such as Vrefl and Vref2. The input end 2 is connected to an output end of a GOA unit 220 (denoted as Nscan1) in a same row, and may be used by the pixel unit 210 to receive a data holding signal (denoted as S1) output by the GOA unit 220, to control a light-emitting diode in the pixel unit to maintain a luminance. The input end S2 is connected to an output end of a GOA unit 230 (denoted as Pscan1) in a same row, and may be used by the pixel unit 210 to receive a data writing control signal (denoted as G1) output by the GOA unit 230, to enable the input end Data of the pixel unit to receive data writing of the DDIC. The data writing is embodied as a data voltage Vdata loaded to the input end Data. The input end Data may be connected to the DDIC, and may be used by the pixel unit to receive data writing (the data voltage Vdata) of the DDIC and adjust light emitting of a light-emitting component. The reset voltage input end may be connected to the DDIC, and may be used by the pixel unit to receive an externally provided reset voltage (for example, the DDIC) and perform reset processing.

For example, the data signal is reset based on a reset voltage of the input end Vrefl (also referred to as a reset voltage Vrefl), and the data signal is restored to a default value, where the default value may be usually set to a low luminance value. For another example, an anode voltage of a light-emitting component (for example, an OLED) in the pixel unit is reset based on a reset voltage of the input end Vref2 (also referred to as a reset voltage Vref2).

[0076] FIG. 3 shows a basic structure of an LPTO pixel unit. As shown in FIG. 3, the pixel unit 210 may include transistors M1 to M7 and a light-emitting component OLED. The transistor M1 is a driving transistor, the transistor M2 is a data input transistor, the transistor M3 is a compensation transistor, the transistors M5 and M6 are light-emitting control transistors, and the transistors M4 and M7 are reset transistors. A control electrode (a gate in the figure) of the transistor M2 is electrically connected to an input end 1 to receive a data writing control signal G1 output by a GOA unit 230. A (drain in the figure) of the transistor M2 is electrically connected to an input end Data to receive data writing (a data voltage Vdata) of a DDIC. A control electrode (a gate in the figure) of the transistor M3 is electrically connected to an input end 2 to receive a row scanning signal S1 (also referred to as a data holding signal) output by a GOA unit 220. Control electrodes of the transistors M4 and M7 are electrically connected to a reset control end Reset to receive a reset control signal, and sources of the transistors M4 and M7 are connected to input ends Vrefl and Vref2 to receive an externally provided reset voltage. Vdd and Vss in FIG. 3 may respectively indicate a positive electrode of a power supply and a negative electrode of the power supply.

[0077] Values of the reset voltage and the data voltage Vdata affect a luminance of the light-emitting component OLED. In this embodiment of this application, the values of the reset voltage and the data voltage Vdata may be adjusted to adjust light emitting of the OLED, thereby improving screen display effect. Detailed descriptions are provided in subsequent embodiments, and are not provided herein.

[0078] The GOA circuit 22 may include M*N cascaded GOA units 220 (denoted as Nscan1). The M*N GOA units 220 may be connected to M enable signal lines, for example, variable frequency enable (variable frequency enable, VFE) signal lines, to receive enable signals. One enable signal line is connected to N cascaded GOA units 220. In the example in FIG. 1, M=4, N=8, and there are 32 Nscan1 in total. 1st Nscan1 to 8th Nscan1 are connected to an enable signal VFE 1, 9th Nscan1 to 16th Nscan1 are connected to an enable signal VFE 2, 17th Nscan1 to 24th Nscan1 are connected to an enable signal VFE 3, and 25th Nscan1 to 32nd Nscan1 are connected to an enable signal VFE 4.

[0079] The cascaded M*N GOA units 220 may indicate that a start vertical (start vertical, STV) signal input end of an $(i+1)^{th}$ GOA unit 220 is connected to an output end of an i^{th} GOA unit 220, that is, an STV signal input of a next GOA unit 220 is affected by an output of a previous GOA unit 220, where i is a positive integer, and $i \leq M*N$. The start vertical (STV) signal is also referred to as a frame start signal. Particularly, as shown in FIG. 3, an STV signal input end of a 1st GOA unit 220 is connected to an STVN signal line, that is, a first row is triggered by a frame start signal STVN. The 1st GOA unit 220 is specifically a 1st GOA unit 220 that is in the M*N GOA units 220 and that is connected to a 1st enable signal, for example, a 1st GOA unit 220 that is connected to VFE 1.

[0080] An output end of one GOA unit 220 may be connected to input ends 2 of P pixel units, and may be configured to output a data holding signal S1 to the P pixel units. In the example in FIG. 1, P=2.

[0081] The GOA circuit 23 may include M*N*P cascaded GOA units 230 (denoted as Pscan1). An output end of one GOA unit 230 may be connected to an input end 1 of one pixel unit 210, and may be configured to output a data writing control signal G1 to the pixel unit 210.

[0082] The cascaded M*N*P GOA units 230 may indicate that an STV signal input end of a $(j+1)^{th}$ GOA unit 230 is connected to an output end of a j^{th} GOA unit 230, that is, an STV signal input of a next GOA unit 230 is affected by an output of a previous GOA unit 230, where j is a positive integer, and $j \leq M*N*P$. Particularly, as shown in FIG. 3, an STV signal input end of a 1st GOA unit 230 is connected to an STVP signal line.

[0083] FIG. 4 briefly shows timing logic of an output signal and an input signal of each component of the display 10.

[0084] VFE signal: The VFE signal is active high. In a data refresh area, the VFE signal maintains a high level. In a data holding area, the VFE signal maintains a low level. When the VFE signal is asserted, a data voltage Vdata can be written into a data pixel unit. When the VFE signal is deasserted, a data voltage cannot be written into a data pixel unit. As shown in FIG. 4, VFE signals on M enable signals appear successively. High-level duration (a pulse width) of one VFE signal may be a*N row scanning times, where a is a positive integer. An i^{th} VFE signal may be N row scanning times later than an $(i-1)^{th}$ VFE signal. A value of N is equal to a quantity of stages of GOA unit 220 connected to one VFE signal line. H indicates a row scanning time, namely, a time required for completing scanning of one row. In FIG. 4, a spacing between two adjacent vertical dashed lines indicates 1H.

[0085] STVN signal: The STVN signal is active high. After a VFE 1 signal, the STVN signal arrives, and may be input to an STV signal input end of a 1st GOA unit 220, to trigger the 1st GOA unit 220 to output a data holding signal S1-1. As shown in FIG. 4, a pulse width of the STVN signal is the same as that of a data holding signal S1 output by each GOA unit 220; and the signal S1-1 is 1H later than the STVN signal. The S1-1 signal is a data holding signal output by the 1st GOA unit 220.

[0086] Data holding signal S1: The data holding signal S1 is also referred to as a row scanning signal. Pulse widths of data holding signals S1 output by GOA units

220 are the same. A data holding signal S1 output by an i^{th} GOA unit 220 is 1H or 2H earlier than a data holding signal S1 output by an $(i+1)^{th}$ GOA unit 220. 1H is used as an example. As shown in FIG. 4, S1-1, S1-2, S1-3, and S1-4 respectively indicate signals S1 output by 1^{st}, 2^{nd}, 3^{rd}, and 4^{th} GOA units 220, where S1-1 is 1H earlier than S1-2, S1-2 is 1H earlier than S1-3, and S1-3 is 1H earlier than S1-4. FIG. 4 shows only timing of S1-1 to S1-4, but timing logic that S1-i is 1H or 2H earlier than S1-(i+1) also exists in a next-stage circuit.

[0087] STVP signal: The STVP signal may be active high or active low. Within duration of a signal S1, the STVP signal arrives, and may be input to an STV signal input end of a 1^{st} GOA unit 230, to trigger the 1^{st} GOA unit 230 to output a data writing control signal G1-1. As shown in FIG. 4, a pulse width of the STVP signal is the same as that of a data writing control signal G1 output by each GOA unit 230, and the signal G1-1 is second duration, for example, 0.5H later than the STVP signal. Pulse widths of the STVP signal and the data writing control signal G1 are equal and are both small, for example, 0.7H.

[0088] Data writing control signal G1: Pulse widths of data writing control signals G1 output by GOA units 230 are the same. A signal G1 output by an $(i+1)^{th}$ GOA unit 230 is also second duration later than a data holding signal G1 output by an i^{th} GOA unit 230. As shown in FIG. 4, G1-1, G1-2, G1-3, G1-4, ..., and G1-8 respectively indicate signals G1 respectively output by 1^{st}, 2^{nd}, 3^{rd} 4^{th}, ..., and 8^{th} GOA units 230. G1-1, G1-2, G1-3, G1-4, ..., and G1-8 arrive in sequence, and there is a difference of second duration between two adjacent signals G1.

[0089] In this embodiment of this application, increasing a quantity M of VFE signals can increase the pulse width of the data holding signal S1. The following relationship exists between the pulse width Y of the VFE signal and the pulse width X of the signal S1: $M*Y \geq X+(M*N-1)*Q$, where M indicates the quantity of VFE signals, N indicates a quantity of GOA units 220 connected to one VFE signal, Q indicates that the data holding signal S1 output by the i^{th} GOA unit 220 is Q row scanning times earlier than the data holding signal S1 output by the $(i+1)^{th}$ GOA unit 220, and a value of Q may be 1, 2, or the like. In this relational expression, M*Y indicates a maximum pulse width that can be covered together by M VFE signals, and X+(M*N-1)*Q indicates a pulse width covered together by the data holding signals S1 output by all stages of GOA units 220 on the M VFE signals.

[0090] A constraint of the relational expression can ensure that all the GOA units 220 connected to the M VFE signal lines can effectively output the signal S1. In addition, a maximum pulse width $X_{max}=M*Y-(M*N-1)*Q$ of the signal S1 may be determined by using the relational expression. It can be learned that greater M indicates greater X_{max}, that is, increasing the quantity of VFE signals can increase the pulse width of the signal S1. In the constraining formula of X_{max}, an implicit condition is further included: Y>Q*N, that is, the pulse width of the VFE signal is greater than a width of a coupling area of the signal S1.

Embodiment 1

[0091] This embodiment provides a partition refresh method of a display. The method may be applied to the display 10 shown in FIG. 1. In this method, a pulse width of a data holding signal S1 output by a GOA unit 220 can be increased, so that data writing into a pixel unit is not interfered by a glitch of the signal S1, to avoid screen horizontal stripes shown in FIG. 5.

[0092] Currently, a display with a partition variable frequency function is prone to generating the screen horizontal stripes shown in FIG. 5.

[0093] It is found through research that, data holding signals S1 output by GOA units 220 connected to a same VFE signal interfere with each other, and a rising edge of a signal S1 output by a subsequent stage of GOA unit 220 causes a glitch of a signal S1 output by a previous stage of GOA unit 220, and the glitch affects data writing into the pixel unit, finally causing a horizontal stripe.

[0094] FIG. 6 is a diagram of signal timing present when the display uses two VFE signal lines. As shown in FIG. 6, when an S1-2 signal arrives, a rising edge of the S1-2 signal causes a glitch of an S1-1 signal at this moment. Similarly, when an S1-3 signal arrives, a rising edge of the S1-3 signal causes glitches of both the S1-1 signal and the S1-2 signal at this moment. The rest may be deduced by analogy. If eight GOA units 220 are connected to one VFE signal line, there are seven glitches in the S1-1 signal, affecting eight row scanning times; and there are six glitches in the S1-2 signal, affecting seven row scanning times. The rest may be deduced by analogy.

[0095] In this specification, a time period in which one signal S1 is affected by a glitch within duration of the signal S1 may be referred to as a coupling area, and a time in which the signal S1 is not affected by a glitch during the duration of the signal S1 may be referred to as a non-coupling area. If a GOA unit 230 outputs a signal G1 in the coupling area, data writing into the pixel unit is infected, and consequently, a horizontal stripe is generated on a screen. As shown in FIG. 6, a coupling area of S1-1 is long, and signals G1-1 and G1-2 appear in the coupling area, which causes a horizontal stripe. A coupling area of S1-2 is also long, and G1-3 and G1-4 appear in the coupling area, which also causes a horizontal stripe. However, a coupling area of S1-3 gradually becomes shorter, and G1-5 and G1-6 do not appear in the coupling area, which does not cause a horizontal stripe. A coupling area of a subsequent signal S1 is shorter, and a signal G1 falls in a non-coupling area, which does not cause a horizontal stripe.

[0096] As shown in FIG. 7, a partition refresh method of a display provided in an embodiment of this application may include the following steps.

[0097] S11: At a moment h, control an initial GOA unit 220 to output a data holding signal S1.

[0098] In other words, at the moment h, a GOA circuit 22 is controlled to start to output the data holding signal S1. The initial GOA unit 220 is a 1st GOA unit 220 in cascaded M*N GOA units 220, and is triggered by an STVN signal to output the data holding signal S1.

[0099] In the cascaded M*N GOA units 220, an i^{th} GOA unit 220 specifically starts to output the data holding signal S1 at a moment h+(i-1)*Q*H, where i is a positive integer, and $i \leq M*N$. Q indicates that an i^{th} first GOA unit outputs the data holding signal Q row scanning times earlier than an $(i+1)^{th}$ first GOA unit, and a value of Q may be a positive integer, for example, 1 or 2. H indicates one row scanning time, and is a time length concept, for example, several microseconds.

[0100] For example, as shown in FIG. 8, the 1st GOA unit 220 starts to output S1-1 at the moment h, a 2nd GOA unit 220 starts to output S1-2 at a moment h+H, a 3rd GOA unit 220 starts to output S1-3 at a moment h+2*H, and a 4th GOA unit 220 starts to output S1-4 at a moment h+3*H.

[0101] In addition, the data holding signal S1 output by each GOA unit 220 may last for X row scanning times, where X is a positive integer, and X>N. In other words, a pulse width of the data holding signal S1 is at least greater than N row scanning times, to ensure that the pulse width of the data holding signal S1 output by each GOA unit 220 includes a non-coupling area, because a longest coupling area of the data holding signal S1 is equal to N row scanning times, and exists within duration of a signal S1 output by a first-stage GOA unit 220 on a VFE signal line.

[0102] For example, as shown in FIG. 8, S1-1 indicates the signal S1 output by the first-stage GOA unit 220 on the VFE signal line, and a coupling area of the signal S1 is the longest coupling area. When eight GOA units 220 are connected to one VFE signal line (that is, N=8), S1-1 has seven glitches, and the longest coupling area is eight row scanning times affected by the seven glitches.

[0103] In this embodiment, M>2, for example, M=4, that is, more enable signal lines are introduced to the display 10. In this way, enable signals may be provided for the cascaded GOA units 220 for a longer time, to provide a condition for increasing the pulse width of the data holding signal S1 and creating the non-coupling area.

[0104] It can be learned from the foregoing calculation formula of the maximum value X_{max} of X that greater X indicates a larger non-coupling area. If a signal G1 output by a GOA unit 230 falls in the non-coupling area, data writing into a pixel unit is not affected by a glitch of the signal S1, and a problem of a horizontal stripe does not occur.

[0105] S12: At a moment k, control an initial GOA unit 230 to output a data writing control signal G1.

[0106] In other words, at the moment k, a GOA circuit 23 starts to output the data writing control signal G1. The initial GOA unit 230 is a 1st GOA unit 230 in cascaded M*N*P GOA units 230, and is triggered by an STVP signal to output the data writing control signal G1.

[0107] The moment k is later than a moment h+N*H, where N*H indicates a length of the longest coupling area, and H indicates one row scanning time, for example, several microseconds. This setting may enable the data writing control signal G1 to appear after the coupling area of the data holding signal S1, so that data writing into the pixel unit is not affected by the glitch of S1, and no screen horizontal stripe appears.

[0108] In addition, the moment k is earlier than a moment h+X*H. As described above, X indicates duration of the data holding signal S1. This setting enables the data writing control signal G1 to be generated before the data holding signal S1 ends, ensuring that data is written normally.

[0109] As shown in FIG. 8, in the cascaded M*N*P GOA units 230, the 1st GOA unit 230 starts to output a data writing control signal G1-1 at the moment k, a 2nd GOA unit 230 starts to output a data writing control signal G1-2 at a moment k+q, and a 3rd GOA unit 230 starts to output a data writing control signal G1-3 at a moment k+2*q. By analogy, a j^{th} GOA unit 230 starts to output a data writing control signal G1 at a moment k+(j-1)*q, where q indicates a time by which the data writing control signal G1 output by the j^{th} GOA unit 230 is later than a data writing control signal G1 output by a $(j-1)^{th}$ GOA unit 230, namely, the second duration.

[0110] Duration of the data writing control signal G1 is short and a pulse width of the data writing control signal G1 is narrow. Two adjacent GOA units 230 may successively output signals G1 within a same row scanning time H. Reference may be made to FIG. 8.

[0111] The partition refresh method of the display provided in this embodiment of this application may further include the following steps.

[0112] The STVN signal is provided at a moment h-Q*H, that is, the STV signal is transmitted to an input end of the initial GOA unit 220, to trigger the initial GOA unit 220 to output the data holding signal S1 at the moment h, where Q indicates that the i^{th} first GOA unit outputs the data holding signal Q row scanning times earlier than the $(i+1)^{th}$ first GOA unit, and a value of Q may be equal to a positive integer, for example, 1 or 2.

[0113] The STVP signal is provided at a moment k-q, that is, an STV signal is transmitted to an input end of the initial GOA unit 230, to trigger the initial GOA unit 230 to output the data writing control signal G1 at the moment k.

[0114] In addition, the method may further include: before a moment h-H, controlling the VFE signal line to start to provide a VFE signal. A VFE signal on each VFE signal line lasts for Y row scanning times (H). For example, as shown in FIG. 8, a 1st VFE signal line is controlled to start to provide a VFE signal at a moment s, a 2nd VFE signal line is controlled to start to provide a VFE signal at a moment s+N, a 3rd VFE signal line is controlled to start to provide a VFE signal at a moment s+2*N, and a 4th VFE signal line is controlled to start to provide a VFE signal at a moment s+3*N. By analogy, a w^{th} VFE signal line starts to provide a VFE signal at a moment s+(w-1)*N, where N indicates a time by which an i^{th} VFE signal is later than an

$(i-1)^{th}$ VFE signal, and a value of N is equal to a quantity of stages of GOA units 220 connected to one VFE signal line.

[0115] The partition refresh method of the display provided in this embodiment of this application may be performed by a DDIC connected to the display 10, or may be performed by a display system including the display 10 and a DDIC, or may be performed by an electronic device including the display 10 and a DDIC.

[0116] This embodiment further provides the following steps, so that a falling edge of the signal S1 is not affected by a falling edge of the VFE signal: controlling, to be equal to or later than a specific time, a time for switching a VFE signal on an M^{th} VFE signal line from a high level to a low level, where the specific time is a time for switching, from a high level to a low level, a signal S1 output by a last GOA unit 220 connected to the VFE signal. In this way, a falling edge of the VFE signal is later than a falling edge of a last-stage signal S1 on the VFE signal line, so that a level drop of S1 is not affected by a drop of VFE, to avoid a problem of a dark line on the screen shown in FIG. 9.

[0117] This requires that the following relationship exists between a pulse width Y of a single VFE signal and a pulse width X of a signal S1 output by a single GOA unit 220: $Y \geq X+(N-1)*Q$, where N indicates a quantity of GOA units 220 connected to one VFE signal, Q indicates that a data holding signal S1 output by an i^{th} GOA unit 220 is Q row scanning times earlier than a data holding signal S1 output by an $(i+1)^{th}$ GOA unit 220, and a value of Q may be 1, 2, or the like. In this relational expression, X+(N-1)*Q indicates a pulse width covered together by data holding signals S1 output by all stages of GOA units 220 on one VFE signal. A constraint of the relational expression can ensure that a falling edge of a VFE signal is later than a falling edge of a signal S1 output by a last-stage GOA unit on the VFE signal line, to avoid a problem of a dark line on the screen.

[0118] The method steps provided in this embodiment may be implemented in combination with other embodiments, for example, in combination with Embodiment 2, to comprehensively resolve more problems in partition frequency conversion of the display.

Embodiment 2

[0119] This embodiment provides a partition refresh method of a display. The method may be applied to the display 10 shown in FIG. 1. Adjusting a reset voltage Vref of a pixel unit can reduce a luminance difference between different screen partitions, to avoid screen flickering.

[0120] FIG. 10 shows a problem of the luminance difference between different screen partitions: A luminance of an area with a lower refresh rate is higher than a luminance of an area with a higher refresh rate. A, B, and C indicate three screen partitions. The problem of the luminance difference is caused by the following reasons: As shown in FIG. 11, when a DDIC writes picture data into the display (a writing frame), a luminance of the display is low; when the DDIC does not write picture data into the display (a holding frame), a luminance of the display is high; at a low refresh rate, for example, 1 Hz, there are significantly more holding frames than writing frames; and at a high refresh rate, for example, 120 Hz, there are significantly more writing frames than holding frames. Therefore, a luminance of a low-refresh-rate area is obviously higher than a luminance of a high-refresh-rate area. In addition, during switching from the saving frame to the writing frame or from the writing frame to the holding frame, the luminance difference causes screen flickering.

[0121] In this embodiment, the luminance difference between different screen partitions is reduced by using the following strategies, which are briefly summarized as follows.

[0122] Strategy 1: During data writing into the pixel unit, Vref of the low-refresh-rate screen area performs voltage bias with reference to Vref of the high-refresh-rate screen area, so that the luminance of the low-refresh-rate screen area is adjusted to the luminance of the high-refresh-rate screen area, and power consumption of the display may be further reduced while screen luminances are unified. Reference may be made to the method shown in FIG. 12.

[0123] Strategy 2: For the high-refresh-rate screen area, Vref of the holding frame performs voltage bias with reference to Vref of the writing frame, so that a high luminance in the holding frame is adjusted to a low luminance in the writing frame, and a screen luminance can be kept without sudden changes during switching between the holding frame and the writing frame, to avoid a problem of screen flickering. Reference may be made to the method shown in FIG. 14.

[0124] Strategy 3: For the low-refresh-rate screen area, Vref of the holding frame performs voltage bias with reference to Vref of the writing frame, so that a high luminance in the holding frame is adjusted to a low luminance in the writing frame, and a screen luminance can be kept without sudden changes during switching between the holding frame and the writing frame, to avoid a problem of screen flickering at a low refresh rate. Reference may also be made to the method shown in FIG. 14.

[0125] As shown in FIG. 12, a partition refresh method of a display provided in this embodiment may include the following steps.

[0126] S21: Determine a time for performing data writing into a pixel unit in a first screen area, namely, a time range of a writing frame.

[0127] For example, when to start to perform data writing may be determined based on a refresh rate, and duration of a next writing frame at a known refresh rate is knowable.

[0128] S22: When performing data writing into the pixel unit in the first screen area, perform first bias processing on a reset voltage Vref of the pixel unit in the first screen area, where Vref after the first bias processing is a reset voltage corresponding to a first reference luminance at a first refresh rate during data writing. In this way, a lumi-

nance of the first screen area with a low refresh rate during data writing may be adjusted to the first reference luminance.

[0129] In this embodiment of this application, the first reference luminance may be less than a luminance corresponding to the reset voltage Vref of the pixel unit in the first screen area at the first refresh rate before the first bias processing, to reduce the luminance of the first screen area with the low refresh rate, and reduce power consumption of the display.

[0130] A luminance and a reset voltage Vref during data writing have different correspondences at different refresh rates. In addition, the correspondence may be further measured and recorded in advance, to adjust the reset voltage during data writing, and unify screen luminances.

[0131] FIG. 13 shows mapping relationships between luminances and Vrefl at 1 Hz and 120 Hz during data writing. As shown in FIG. 13, at the two refresh rates, during data writing, greater Vrefl (an absolute value) indicates a greater luminance. Generally, for same Vrefl, a luminance at 1 Hz is higher than a luminance at 120 Hz. During data writing, at a same luminance, Vrefl of a pixel unit in a low-refresh-rate area is smaller than Vrefl of a pixel unit in a high-refresh-rate area. For example, during data writing, to implement a reference luminance of 8.0 nits, Vrefl at 120 Hz is set to approximately 1.0 V, and Vrefl at 1 Hz is set to approximately 0.5 V. Values in FIG. 13 are merely used for illustration to facilitate understanding of the solution by a reader, and should not constitute a limitation on this embodiment of this application.

[0132] Similarly, during data writing, there are also mapping relationships between luminances and reset voltages Vref2 at different refresh rates.

[0133] FIG. 13 shows, by using a curve diagram, correspondences between luminances and reset voltages Vref at different refresh rates during data writing, where one curve is equivalent to one mapping table of luminances and reset voltages Vref. This is not limited thereto. The correspondence may be further recorded in a mapping table. A data representation form of the correspondence is not limited in this embodiment of this application.

[0134] In this embodiment of this application, the first reference luminance may be specifically a luminance corresponding to a first reset voltage at a second refresh rate during data writing, and the first reset voltage is a reset voltage of a pixel unit in a second screen area during data writing into the second screen area under refresh at the second refresh rate, and may be measured by a DDIC. The first refresh rate is lower than the second refresh rate. In this way, the luminance of the first screen area with the low refresh rate may be adjusted to a luminance of the second screen area with a high refresh rate, to unify luminances of partitions with different refresh rates and reduce a luminance difference.

[0135] The second screen area may be specifically a screen area with a highest refresh rate, which is more conducive to reducing power consumption of the display.

[0136] The partition refresh method of the display provided in this embodiment may further include the following steps: S23: Determine a refresh rate of each area on a screen; S24: Select the reset voltage of the pixel unit in the second screen area as the first reset voltage; S25: Search a first mapping table for a luminance corresponding to the first reset voltage, and determine the found luminance as the first reference luminance; and S26: Search a second mapping table for a reset voltage corresponding to the first reference luminance, and determine the found reset voltage as the reset voltage Vref after the first bias processing, which is used in step S22.

[0137] The first mapping table may record luminances present when the pixel unit uses different reset voltages Vref during data writing at the second refresh rate. The second mapping table may record luminances present when the pixel unit uses different reset voltages Vref during data writing at the first refresh rate.

[0138] The first reference luminance may not be a luminance of any screen partition, but is only default luminance. In this way, a luminance of each screen partition may be adjusted to the empirical luminance, to implementing a uniform screen luminance.

[0139] As shown in FIG. 14, a partition refresh method of a display provided in this embodiment may include the following steps.

[0140] S31: Determine a time for skipping performing data writing into a pixel unit in a third screen area, namely, a time range of a holding frame, where a refresh rate of the third screen area is a third refresh rate.

[0141] For example, when to skip performing data writing may be determined based on the third refresh rate, and duration of a next holding frame at a known refresh rate is fixed and known.

[0142] S32: When skipping performing data writing into the pixel unit in the third screen area, perform second bias processing on a reset voltage Vref of the pixel unit in the third screen area, where Vref after the second bias processing is a reset voltage corresponding to a second reference luminance at the third refresh rate during data holding.

[0143] The second reference luminance may be a luminance corresponding to a second reset voltage at the third refresh rate during data writing. The second reset voltage is a reset voltage during data writing into the third screen area at the third refresh rate, and may be measured by a DDIC. In this way, a luminance of the third screen area during data holding may be adjusted to a luminance of the third screen area during data writing, and the luminance of the third screen area may be kept without sudden changes during switching between data holding and data writing, to avoid screen flickering.

[0144] FIG. 15 shows, by using a curve diagram, correspondences between luminances and reset voltages Vref at different refresh rates during data holding. One curve is equivalent to one mapping table of luminances and reset voltages Vref. The correspondence may be

measured and recorded in advance, to adjust the reset voltage during data holding. Based on the correspondence, a luminance value corresponding to a reset voltage at a specific refresh rate during data writing may be determined, and a reset voltage corresponding to a luminance at a specific refresh rate during data writing may also be determined.

[0145] The partition refresh method of the display provided in this embodiment may further include the following steps: S33: Determine a time for performing data writing into the third screen area; S34: Use, as the second reset voltage, a reset voltage during data writing into the third screen area at the third refresh rate; S35: Search a third mapping table for a luminance corresponding to the second reset voltage, and determine the found luminance as the second reference luminance; and S36: Search a fourth mapping table for a reset voltage corresponding to the second reference luminance, and determine the found reset voltage as the reset voltage Vref after the second bias processing, which is used in step S32.

[0146] The third mapping table may record luminances present when the pixel unit uses different reset voltages Vref during data writing at the third refresh rate. The fourth mapping table may record luminances present when the pixel unit uses different reset voltages Vref during data holding at the third refresh rate.

[0147] The third screen area may be a low-refresh-rate screen area, for example, the foregoing first screen area. In this case, the third refresh rate is a low refresh rate and may be the same as the foregoing first refresh rate, and the third mapping table may be the same as the foregoing second mapping table. The third screen area may alternatively be a high-refresh-rate screen area, for example, the foregoing second screen area. In this case, the third refresh rate is a high refresh rate and may be the same as the foregoing second refresh rate, and the fourth mapping table may be the same as the foregoing first mapping table.

[0148] When the third screen area is a low-refresh-rate screen area, the second reset voltage may further be the reset voltage after the first bias processing in step S22. That is, for a low-refresh-rate screen area, bias processing (namely, first bias processing) may be first performed on a reset voltage once with reference to a first reference luminance (for example, a luminance of a high-refresh-rate screen area) during data writing, to resolve a problem that a luminance of the low-refresh-rate area is different from that of the high-refresh-rate area during data writing, and reduce power consumption; and then bias processing (namely, first bias processing) is performed on the reset voltage again with reference to the second reference luminance (for example, a luminance during data writing), to resolve a problem of different luminances during data holding and data writing, and reduce power consumption.

[0149] Step S31 and step S32 may be combined with the method shown in FIG. 12, and a problem of a luminance difference between screen partitions and a problem of screen flickering are resolved.

[0150] In this embodiment of this application, performing bias processing on a reset voltage is adjusting a value of the reset voltage, to adjust the reset voltage to a target voltage that can implement a reference luminance, for example, the reset voltage corresponding to the first reference luminance at the first refresh rate during data writing mentioned in step S22, and the reset voltage corresponding to the second reference luminance at the first refresh rate during data holding mentioned in step S22. The reset voltage may include one or more of the foregoing Vrefl and Vref2, and is not limited thereto. The reset voltage may further include another reset voltage, which specifically depends on a circuit structure of the pixel unit.

[0151] FIG. 16 shows an example of bias values that are of reset voltages and that are used in areas with different refresh rates to implement a same luminance during data writing and data holding. As shown in FIG. 16, during data writing, to implement a same luminance, a bias value of Vrefl of a low-refresh-rate area relative to Vrefl of a high-refresh-rate area is $\Delta V11$; in a same high-refresh-rate area, to keep a luminance without sudden changes, a bias value of Vrefl during data holding relative to Vrefl during data writing is $\Delta V12$; and in a same low-refresh-rate area, to keep a luminance without sudden changes, a bias value of Vrefl during data holding relative to Vrefl during data writing is $\Delta V13$. As shown in FIG. 16, $\Delta V13$ is determined based on Vrefl after first bias processing ($\Delta V11$ is added) during data writing, to resolve a problem of a luminance difference between the low refresh area and the high-refresh-rate area during data writing and a problem of a luminance sudden change in the low refresh area during data holding and data writing. FIG. 16 also shows bias processing of Vref2. Reference may be made to Vrefl. Details are not described herein again. FIG. 16 is merely used to explain this embodiment of this application. A quantity of screen partitions, a quantity of reset voltages, a bias value, a bias direction, and the like shown in FIG. 16 do not constitute a limitation on this embodiment of this application. In this embodiment of this application, the bias value may range from -10 V to +10 V.

[0152] In this embodiment of this application, for pixel units in entire screen areas, a quantity of times of performing bias processing (including first bias processing and second bias processing) on a reset voltage in a unit time depends on a quantity of screen partitions, a quantity of reset voltages, and a quantity of holding frames.

[0153] The partition refresh method of the display provided in this embodiment may be performed by a display system including the display 10 and a DDIC, or executed by an electronic device including the display 10 and a DDIC.

Embodiment 3

[0154] This embodiment provides a partition refresh method of a display. The method may be applied to the display 10 shown in FIG. 1. Adjusting a data voltage Vdata of a pixel unit can reduce a luminance difference between a high-refresh-rate area and a low-refresh-rate area at a same gray scale.

[0155] Luminances of pixel units at a same gray scale in areas with different refresh rates may be different. As a result, presentation effect of a same gray scale in different screen areas is different. For example, a pixel unit a in the high-refresh-rate area and a pixel unit b in the low-refresh-rate area need to present a same gray scale, but actual luminance values of a and b are inconsistent, which affects overall expression of a picture gray scale.

[0156] In this embodiment, a luminance difference of a same gray scale in areas with different refresh rates are reduced by using the following strategy, which is briefly summarized as follows: For a same gray scale, Vdata of the low-refresh-rate screen area performs voltage bias with reference to Vdata of the high-refresh-rate screen area, so that performance of the same gray scale in the low-refresh-rate area is consistent with that in the high-refresh-rate area, and power consumption of the display may further be reduced. Reference may be made to the method shown in FIG. 17.

[0157] As shown in FIG. 17, a partition refresh method of a display provided in this embodiment may include the following steps.

[0158] S41: Determine a gray scale of a pixel unit in a first screen area.

[0159] For example, a gray scale of a pixel unit in each screen area may be determined based on gray scale information of a to-be-refreshed picture. A gray scale of a pixel is a gray scale value of the pixel, and indicates a luminance of the pixel presented in a picture. This step may be performed by a DDIC, or a SoC may transmit a result to a DDIC after performing this step.

[0160] S42: When performing data writing into a first pixel unit in the first screen area, perform third bias processing on a data voltage Vdata of the first pixel unit, where Vdata after the third bias processing is a data voltage Vdata corresponding to a third reference luminance at a first refresh rate during data writing, and the first pixel unit is a pixel unit whose gray scale is a first gray scale in the first screen area.

[0161] The third reference luminance is a luminance corresponding to first Vdata at a second refresh rate, and the first Vdata is Vdata during data writing into a second pixel unit at the second refresh rate, and may be measured by the DDIC. The second pixel unit is a pixel unit at the first gray scale in a second screen area, a refresh rate of the second screen area is the second refresh rate, and the second refresh rate is greater than the first refresh rate. In this way, during data writing, a luminance of a gray scale in the low-refresh-rate area may be adjusted to a luminance of the gray scale in the high-refresh-rate area, so that a same gray scale has consistent performance in the low-refresh-rate area and the high-refresh-rate area, and power consumption of the display may be further reduced.

[0162] FIG. 18 shows, by using a curve diagram, correspondences between luminances and data voltages Vdata at different refresh rates during data writing. One curve is equivalent to one mapping table of luminances and data voltages Vdata. The correspondence may be measured and recorded in advance, to adjust the data voltage Vdata. Based on the correspondence, a luminance value corresponding to a data voltage Vdata at a specific refresh rate may be determined, and a data voltage Vdata corresponding to a luminance at a specific refresh rate may also be determined.

[0163] The partition refresh method of the display provided in this embodiment may further include the following steps: S43: Determine a refresh rate of each area on a screen; S44: Select a pixel unit at the first gray scale (namely, the foregoing second pixel unit) from the second screen area, and use Vdata of the pixel unit as the first Vdata; S45: Search a fifth mapping table for a luminance corresponding to the first Vdata, and determine the found luminance as the third reference luminance; and S46: Search a sixth mapping table for Vdata corresponding to the third reference luminance, and determine the found Vdata as the Vdata after the third bias processing, which is used in step S42.

[0164] The fifth mapping table may record luminances present when the pixel unit uses different Vdata during data writing at the second refresh rate. The sixth mapping table may record luminances present when the pixel unit uses different Vdata during data writing at the first refresh rate.

[0165] In this embodiment of this application, performing bias processing on the data voltage Vdata is adjusting a value of the data voltage Vdata, to adjust the data voltage Vdata to a target voltage that can implement a reference luminance, for example, the data voltage Vdata corresponding to the third reference luminance at the first refresh rate during data writing mentioned in step S42.

[0166] FIG. 19 shows an example of bias values that are of Vdata and that are used by pixel units that implement a same gray scale in areas with different refresh rates. As shown in FIG. 19, to implement a gray scale 1, a bias value of Vdata in a low-refresh-rate area relative to Vdata in a high-refresh-rate area is $\Delta V1$; to implement a gray scale 2, a bias value of Vdata in the low-refresh-rate area relative to Vdata in the high-refresh-rate area is $\Delta V2$; to implement a gray scale 3, a bias value of Vdata in the low-refresh-rate area relative to Vdata in the high-refresh-rate area is $\Delta V3$; and to implement a gray scale 4, a bias value of Vdata in the low-refresh-rate area relative to Vdata in the high-refresh-rate area is $\Delta V4$. FIG. 19 is merely used to explain this embodiment of this application. A quantity of screen partitions, a quantity of gray scales, a bias value, a bias direction, and the like

shown in FIG. 19 do not constitute a limitation on this embodiment of this application. In this embodiment of this application, the bias value of the data voltage may range from -10 V to +10 V.

[0167] In this embodiment of this application, for pixel units in entire screen areas, a quantity of times of performing bias processing on Vdata in a unit time depends on a quantity of screen partitions and a quantity of gray scales.

[0168] The partition refresh method of the display provided in this embodiment may be performed by a display system including the display 10 and a DDIC, or executed by an electronic device including the display 10 and a DDIC.

Embodiment 4

[0169] This embodiment provides a partition refresh method of a display. The method may be applied to the display 10 shown in FIG. 1. Adjusting a data voltage Vdata of a pixel unit can avoid screen flickering.

[0170] In this embodiment, screen flickering is avoided by using the following strategies, which are briefly summarized as follows.

[0171] Strategy 1: For a high-refresh-rate screen area, Vdata of a holding frame performs voltage bias with reference to Vdata of a writing frame, so that a high luminance in the holding frame is adjusted to a low luminance in the writing frame, and a screen luminance can be kept without sudden changes during switching between the holding frame and the writing frame, to avoid a problem of screen flickering. Reference may be made to the method shown in FIG. 20.

[0172] Strategy 2: For a low-refresh-rate screen area, Vdata of a holding frame performs voltage bias with reference to Vdata of a writing frame, so that a high luminance in the holding frame is adjusted to a low luminance in the writing frame, and a screen luminance can be kept without sudden changes during switching between the holding frame and the writing frame, to avoid a problem of screen flickering. Reference may also be made to the method shown in FIG. 20.

[0173] As shown in FIG. 20, a partition refresh method of a display provided in this embodiment may include the following steps.

[0174] S51: Determine a time for skipping performing data writing into a pixel unit in a fourth screen area, namely, a time range of a holding frame, where a refresh rate of the fourth screen area is a fourth refresh rate.

[0175] For example, when to skip performing data writing may be determined based on the fourth refresh rate, and duration of a next holding frame at a known refresh rate is knowable.

[0176] S52: When skipping performing data writing into the pixel unit in the fourth screen area, perform fourth bias processing on a data voltage Vdata of a third pixel unit in the fourth screen area, where Vdata after the fourth bias processing is a data voltage Vdata corresponding to a fourth reference luminance at the fourth refresh rate during data holding.

[0177] The fourth reference luminance may be a luminance corresponding to second Vdata at the fourth refresh rate during data writing into the fourth screen area. The second Vdata is Vdata during data writing into the third pixel unit at the fourth refresh rate, and may be measured by a DDIC. In this way, a luminance of the third pixel unit during data holding may be adjusted to a luminance of the third pixel unit during data writing, and the luminance of the third pixel unit may be kept without sudden changes during switching between data holding and data writing, to avoid screen flickering.

[0178] Gray scales of different pixel units in the fourth screen area may be different, and Vdata of different pixel units is also different. Therefore, in this embodiment of this application, bias processing is specifically performed, in a unit of a pixel unit, on Vdata during data holding relative to Vdata during data writing.

[0179] FIG. 21 shows, by using a curve diagram, correspondences between luminances and data voltages Vdata at different refresh rates during data holding. One curve is equivalent to one mapping table of luminances and data voltages Vdata. The correspondence may be measured and recorded in advance, to adjust the data voltage during data holding. Based on the correspondence, a luminance value corresponding to a data voltage at a specific refresh rate during data holding may be determined, and a data voltage corresponding to a luminance at a specific refresh rate during data holding may also be determined.

[0180] The partition refresh method of the display provided in this embodiment may further include the following steps: S53: Determine a time for skipping performing data writing into the fourth screen area; S54: Use a data voltage during data writing into the fourth screen area at the fourth refresh rate as the second Vdata; S55: Search a seventh mapping table for a luminance corresponding to the second Vdata, and determine the found luminance as the fourth reference luminance; and S56: Search an eighth mapping table for a data voltage corresponding to the fourth reference luminance, and determine the found data voltage as the data voltage Vref after the fourth bias processing, which is used in step S52.

[0181] The seventh mapping table may record luminances present when the pixel unit uses different data voltages Vdata during data writing at the fourth refresh rate. The eighth mapping table may record luminances present when the pixel unit uses different data voltages Vdata during data holding at the fourth refresh rate.

[0182] The fourth screen area may be a low-refresh-rate screen area, for example, the foregoing first screen area. In this case, the fourth refresh rate is a low refresh rate and may be the same as the foregoing first refresh rate, and the seventh mapping table may be the same as the foregoing sixth mapping table. The fourth screen area may alternatively be a high-refresh-rate screen area, for example, the foregoing second screen area. In this case,

the fourth refresh rate is a high refresh rate and may be the same as the foregoing second refresh rate, and the eighth mapping table may be the same as the foregoing fifth mapping table.

[0183] When the fourth screen area is a low-refresh-rate screen area, the second Vdata may further be the data voltage after the third bias processing in step S42. That is, for a low-refresh-rate screen area, bias processing (namely, third bias processing) may be first performed on a data voltage once with reference to a third reference luminance (for example, a luminance of a high-refresh-rate screen area) during data writing, to resolve a problem that a luminance of the low-refresh-rate area is different from that of the high-refresh-rate area during data writing, and reduce power consumption; and then bias processing (namely, fourth bias processing) is performed on the data voltage again with reference to the fourth reference luminance (for example, a luminance during data writing), to resolve a problem of different luminances during data holding and data writing, and reduce power consumption.

[0184] Step S51 and step S52 may be combined with the method shown in FIG. 17, and a problem of a luminance difference between screen partitions and a problem of screen flickering are resolved.

[0185] FIG. 22 shows an example of bias values that are of data voltages Vdata and that are used in areas with different refresh rates to implement a same luminance during data writing and data holding. As shown in FIG. 22, in a same high-refresh-rate area, to keep a luminance without sudden changes, a bias value of Vdata during data holding relative to Vdata during data writing is $\Delta V1$. In FIG. 21, during data writing, Vdata in a low-refresh-rate area may be the data voltage after the third bias processing in step S42. FIG. 22 further shows that during data holding, a bias value of Vdata of the low-refresh-rate area relative to Vdata of the high-refresh-rate area is $\Delta V2$, to unify luminances of screen areas with different refresh rates during data holding. During data writing, Vdata reflects a gray scale difference. During data holding, Vdata does not reflect the gray scale difference. $\Delta V1$ may be a difference between Vdata during data holding and highest Vdata (for example, Vdata of a 0 gray-scale pixel) during data writing. FIG. 22 is merely used to explain this embodiment of this application. A quantity of screen partitions, a quantity of gray scales, a bias value, a bias direction, and the like shown in FIG. 22 do not constitute a limitation on this embodiment of this application. In this embodiment of this application, the bias value of the data voltage may range from -10 V to +10 V.

[0186] In this embodiment of this application, for pixel units in entire screen areas, a quantity of times of performing bias processing on Vdata in a unit time depends on a quantity of screen partitions, a quantity of gray scales, and a quantity of holding frames.

[0187] The foregoing method embodiments may be combined with each other, to comprehensively resolve more problems generated in partition frequency conversion of the display.

[0188] Based on the partition refresh method of the display provided in the foregoing embodiments, the following describes a display system and an electronic device that are provided in embodiments of this application.

[0189] **FIG. 23 shows a display system 60 according to an embodiment of this application.** As shown in FIG. 23, the display system 60 may include a display 61 and a control circuit 62.

[0190] The display 61 may include a plurality of pixel units. The display 61 may be an organic light-emitting diode (OLED) display panel, where each pixel unit includes an OLED. The display 61 may be the display 10 described in the embodiment in FIG. 1.

[0191] The control circuit 62 may include a display driver circuit, for example, a DDIC, configured to control and drive the display 61 to perform display. A main function of the DDIC is to send a drive signal and data to the display 61 in a form of electrical signal, so that image information is presented on the display 61 through control on a luminance and a color. The control circuit 62 may further include a circuit part for timing control, for example, a time controller (time controller, TCON). The time controller may set timing of a control signal and a data signal, and transmit the control signal and the data signal to the display driver circuit based on the timing. The control signal may be, for example, the VFE signal, the STVP signal, or the STVN signal mentioned in the foregoing method embodiments. Once timing of the STVP signal and the STVN signal are determined, timing of the signal S1 output by the GOA unit 220 and the signal G1 output by the GOA unit 230 is also determined.

[0192] A storage unit may be further disposed in the control circuit 62, to store a code instruction of the partition refresh method of the display provided in embodiments of this application. When the code instruction is reread from the storage unit and the code instruction is run, the display system 60 may perform the method.

[0193] The control circuit 62 may be implemented by hardware, software, or a combination of hardware and software, and may be implemented by, for example, a digital logic circuit and a register that perform functions described in the foregoing method embodiments. The control circuit 62 may be implemented as one or more chips. When the control circuit 62 is implemented as a chip, various functions of the control circuit 62 are integrated into the chip. When the control circuit 62 is implemented as a plurality of chips, for example, a chip system, various functions of the control circuit 62 may be separately integrated into different independent chips.

[0194] **FIG. 24 shows an electronic device 100 according to an embodiment of this application.**

[0195] In this embodiment of this application, a device type of the electronic device 100 may be any one of a mobile phone, a tablet computer, a handheld computer, a desktop computer, a laptop computer, an ultra-mobile

personal computer (ultra-mobile personal computer, UMPC), a netbook, a cellular phone, a personal digital assistant (personal digital assistant, PDA), a smart home device such as a smart large screen or a smart speaker, a wearable device such as a smart band, a smart watch, or smart glasses, an extended reality (extended reality, XR) device such as an augmented reality (augmented reality, AR) device, a virtual reality (virtual reality, VR) device, or a hybrid reality (mixed reality, MR) device, a vehicle-mounted device, a smart city device, or the like.

[0196] As shown in FIG. 24, the electronic device 100 may include: a processor 110, a memory 120, a display 130, a display driver integrated circuit (display driver integrated circuit, DDIC) 140, an antenna 1, an antenna 2, a mobile communication module 150, a wireless communication module 160, an audio module 170, a speaker 170A, a receiver 170B, a microphone 170C, a headset jack 170D, a sensor module 180, a button 190, a motor 191, an indicator 192, a camera 193, a subscriber identity module (subscriber identity module, SIM) card interface 195, and the like. The sensor module 180 may include a gyroscope sensor 180B, an acceleration sensor 180E, a touch sensor 180K, and the like. Components in the electronic device 100 may be connected to each other through a bus.

[0197] There may be one or more processors 110, and the processors 110 may be integrated into an integrated circuit of a system on chip (system on chip, SoC). The SoC is a system-on-chip. The processor 110 may include a central processing unit (central processing unit, CPU), a graphics processing unit (graphic processing unit, GPU), and a display driver integrated circuit (DDIC). The CPU may be an application processor (application processor, AP). The CPU and the GPU may be configured to render and synthesize a picture to be sent to the display 130 for display. The processor 110 may further include a neural-network processing unit (neural-network processing unit, NPU), a modem processor, and the like.

[0198] The processor 110 may include one or more interfaces, for example, an inter-integrated circuit (inter-integrated circuit, I2C) interface, an inter-integrated circuit sound (inter-integrated circuit sound, I2S) interface, a pulse code modulation (pulse code modulation, PCM) interface, a universal asynchronous receiver/transmitter (universal asynchronous receiver/transmitter, UART) interface, a mobile industry processor interface (mobile industry processor interface, MIPI), a general-purpose input/output (GPIO) interface, a subscriber identity module (subscriber identity module, SIM) interface, and/or a universal serial bus (universal serial bus, USB) port.

[0199] A cache may be disposed in the processor 110, and may be configured to store instructions or data that is recently used or cyclically used by the processor 110. If the processor 110 needs to use the instructions or the data again, the instructions or the data may be directly invoked from the cache. This can reduce a waiting time of the processor 110, and improve program running efficiency.

[0200] The memory 120 may include a program storage area and a user data storage area. The program storage area may store an operating system and one or more applications (such as a game application), and the data storage area may store data (such as a photo and a contact) created by a user in a process of using the electronic device 100. The memory 120 may be a high-speed random access memory, or may be a non-volatile memory, for example, a magnetic disk, a flash memory, or a universal flash storage (universal flash storage, UFS). Alternatively, the memory 120 may be an external storage card, for example, a micro SD card.

[0201] The memory 120 may further store a code instruction of the partition refresh method of the display provided in embodiments of this application. When the processor 110 reads the code instruction from the memory 120 and runs the code instruction, the electronic device 100 may perform the method.

[0202] Alternatively, the memory 120 may be integrated into the integrated circuit of the SoC together with the processor 110.

[0203] The electronic device 100 may implement a display function by using the SoC, the DDIC 140, the display 130, and the like.

[0204] The display 130 may have a partition variable frequency function, and may be the display 10 described in the foregoing embodiments. The display 130 may include a display panel, a timing controller (TCON), and the like. The display panel may include a plurality of pixel units, and the display panel may be an organic light-emitting diode (OLED) display panel. Each pixel unit includes an OLED. The TCON is mainly configured to connect the GPU or the SoC to the display panel. After receiving image data or a control signal transmitted by the GPU or the SoC, the TCON sets timing of a control signal and a data signal based on related data or a related signal, and transmits the control signal and the data signal to a display driver circuit according to the timing, to drive the display panel to perform graphic display.

[0205] The display driver integrated circuit (DDIC) 140 may be used as a control core of the display 130, to drive the display 130 to work, and receive data from the SoC (the processor 110), for example, image data and some instructions. The DDIC 140 may send a drive signal and data to the display panel of the display 130 in a form of electrical signal, to control a luminance and a color of a screen, so that image information such as a letter and an image is displayed on the screen, and screen refresh is completed.

[0206] Image data that is of a to-be-displayed picture and that is sent by the SoC to the DDIC 140 may be sent to a frame buffer (Frame Buffer) for storage, to complete sending for display (or referred to as image sending). Then, the DDIC 140 fetches the image data from the frame buffer and drives the display 130 to display.

[0207] A wireless communication function of the electronic device 100 may be implemented through the an-

tenna 1, the antenna 2, the mobile communication module 150, the wireless communication module 160, the modem processor, the baseband processor, and the like.

[0208] The antenna 1 and the antenna 2 are configured to transmit and receive an electromagnetic wave signal. Each antenna in the electronic device 100 may be configured to cover one or more communication frequency bands. Different antennas may be further reused, to improve antenna utilization. For example, the antenna 1 may be reused as a diversity antenna in a wireless local area network. In some other embodiments, the antenna may be used in combination with a tuning switch.

[0209] The mobile communication module 150 may provide a wireless communication solution that is applied to the electronic device 100 and that includes 2G/3G/4G/5G or the like. The mobile communication module 150 may include at least one filter, a switch, a power amplifier, a low noise amplifier (low noise amplifier, LNA), and the like. The mobile communication module 150 may receive an electromagnetic wave through the antenna 1, perform processing such as filtering or amplification on the received electromagnetic wave, and transmit a processed electromagnetic wave to the modem processor for demodulation. The mobile communication module 150 may further amplify a signal modulated by the modem processor, and convert an amplified signal into an electromagnetic wave for radiation through the antenna 1. In some embodiments, at least some functional modules of the mobile communication module 150 may be disposed in the processor 110. In some embodiments, at least some functional modules of the mobile communication module 150 and at least some modules of the processor 110 may be disposed in a same component.

[0210] The modem processor may include a modulator and a demodulator. The modulator is configured to modulate a to-be-sent low-frequency baseband signal into a medium-high-frequency signal. The demodulator is configured to demodulate a received electromagnetic wave signal into a low-frequency baseband signal. Then, the demodulator transmits the low-frequency baseband signal obtained through demodulation to the baseband processor for processing. The low-frequency baseband signal is processed by the baseband processor and then transmitted to the application processor. The application processor outputs a sound signal through an audio device (which is not limited to the speaker 170A, the receiver 170B, or the like), or displays an image or a video on the display 130. In some embodiments, the modem processor may be an independent component. In some other embodiments, the modem processor may be independent of the processor 110, and may be disposed in a same component as the mobile communication module 150 or another functional module.

[0211] The wireless communication module 160 may provide a wireless communication solution that is applied to the electronic device 100, and that includes a wireless local area network (wireless local area network, WLAN) (for example, a wireless fidelity (wireless fidelity, Wi-Fi) network), Bluetooth (Bluetooth, BT), a global navigation satellite system (global navigation satellite system, GNSS), frequency modulation (frequency modulation, FM), a near field communication (near field communication, NFC) technology, an infrared (infrared, IR) technology, and the like. The wireless communication module 160 may be one or more components integrating at least one communication processing module. The wireless communication module 160 receives an electromagnetic wave through the antenna 2, performs frequency modulation and filtering on an electromagnetic wave signal, and sends a processed signal to the processor 110. The wireless communication module 160 may further receive a to-be-sent signal from the processor 110, perform frequency modulation and amplification on the signal, and convert a processed signal into an electromagnetic wave for radiation through the antenna 2.

[0212] In some embodiments, in the electronic device 100, the antenna 1 is coupled to the mobile communication module 150, and the antenna 2 is coupled to the wireless communication module 160, so that the electronic device 100 can communicate with a network and another device by using a wireless communication technology. The wireless communication technology may include a global system for mobile communications (global system for mobile communications, GSM), a general packet radio service (general packet radio service, GPRS), code division multiple access (code division multiple access, CDMA), wideband code division multiple access (wideband code division multiple access, WCDMA), time-division code division multiple access (time-division code division multiple access, TD-SCDMA), long term evolution (long term evolution, LTE), BT, a GNSS, a WLAN, NFC, FM, an IR technology, and/or the like. The GNSS may include a global positioning system (global positioning system, GPS), a global navigation satellite system (global navigation satellite system, GLONASS), a BeiDou navigation satellite system (BeiDou navigation satellite system, BDS), a quasi-zenith satellite system (quasi-zenith satellite system, QZSS), and/or a satellite based augmentation system (satellite based augmentation system, SBAS).

[0213] The electronic device 100 may implement an image shooting function by using the ISP, the camera 193, the video codec, the GPU, the display 130, the application processor, and the like.

[0214] The ISP is configured to process data fed back by the camera 193. For example, during photographing, a shutter is pressed, and light is transmitted to a photosensitive element of the camera through a lens. An optical signal is converted into an electrical signal, and the photosensitive element of the camera transmits the electrical signal to the ISP for processing, to convert the electrical signal into a visible image. The ISP may further perform algorithm optimization on noise, brightness, and complexion of the image. The ISP may further optimize parameters such as exposure and a color temperature of

an image shooting scene. In some embodiments, the ISP may be disposed in the camera 193.

[0215] The camera 193 is configured to capture a static image or a video. An optical image of an object is generated through a lens, and is projected onto a photosensitive element. The photosensitive element may be a charge-coupled device (charge-coupled device, CCD) or a complementary metal-oxide-semiconductor (complementary metal-oxide-semiconductor, CMOS) phototransistor. The photosensitive element converts an optical signal into an electrical signal, and then transmits the electrical signal to the ISP to convert the electrical signal into a digital image signal. The ISP outputs the digital image signal to the DSP for processing. The DSP converts the digital image signal into an image signal in a standard format, for example, RGB or YUV. In some embodiments, the electronic device 100 may include one or N cameras 193, where N is a positive integer greater than 1.

[0216] The digital signal processor is configured to process a digital signal, and may process another digital signal in addition to the digital image signal. For example, when the electronic device 100 selects a frequency, the digital signal processor is configured to perform Fourier transform and the like on frequency energy.

[0217] The video codec is configured to compress or decompress a digital video. The electronic device 100 may support one or more video codecs. In this way, the electronic device 100 may play or record videos in a plurality of coding formats, for example, moving picture experts group (moving picture experts group, MPEG)-1, MPEG-2, MPEG-3, and MPEG-4.

[0218] The NPU is a neural-network (neural-network, NN) computing processor. The NPU quickly processes input information by referring to a structure of a biological neural network, for example, a transfer mode between human brain neurons, and may further continuously perform self-learning. The NPU may be used to implement applications such as intelligent cognition of the electronic device 100, for example, image recognition, facial recognition, voice recognition, and text understanding.

[0219] The electronic device 100 may implement an audio function, for example, music playing and recording, by using the audio module 170, the speaker 170A, the receiver 170B, the microphone 170C, the headset jack 170D, the application processor, and the like.

[0220] The audio module 170 is configured to convert digital audio information into an analog audio signal for output, and is also configured to convert analog audio input into a digital audio signal. The audio module 170 may be further configured to encode and decode an audio signal. In some embodiments, the audio module 170 may be disposed in the processor 110, or some functional modules of the audio module 170 are disposed in the processor 110.

[0221] The speaker 170A, also referred to as a "loudspeaker", is configured to convert an audio electrical signal into a sound signal. The electronic device 100 may be used for listening to music or answering a call in a hands-free mode through the speaker 170A.

[0222] The receiver 170B, also referred to as an "earpiece", is configured to convert an audio electrical signal into a sound signal. When a call is answered or voice information is received through the electronic device 100, the receiver 170B may be put close to a human ear to listen to a voice.

[0223] The microphone 170C, also referred to as a "mike" or a "mic", is configured to convert a sound signal into an electrical signal. When making a call or sending voice information, a user may make a sound near the microphone 170C through a mouth of the user, to input a sound signal to the microphone 170C. At least one microphone 170C may be disposed in the electronic device 100. In some other embodiments, two microphones 170C may be disposed in the electronic device 100, to collect a sound signal and further implement a noise reduction function. In some other embodiments, three, four, or more microphones 170C may alternatively be disposed in the electronic device 100, to collect a sound signal, implement noise reduction, identify a sound source, implement a directional recording function, and the like.

[0224] The headset jack 170D is configured to connect to a wired headset. The headset jack 170D may be a USB port, or may be a 3.5 mm open mobile electronic device platform (open mobile terminal platform, OMTP) standard interface, or a cellular telecommunications industry association of the USA (cellular telecommunications industry association of the USA, CTIA) standard interface.

[0225] The button 190 includes a power button, a volume button, and the like. The button 190 may be a mechanical button, or may be a touch button. The electronic device 100 may receive button input, and generate button signal input related to user setting and function control of the electronic device 100. The motor 191 may generate a vibration prompt. The SIM card interface 195 is configured to connect to a SIM card. The SIM card may be inserted into the SIM card interface 195 or removed from the SIM card interface 195, to implement contact with or separation from the electronic device 100.

[0226] The structure shown in FIG. 24 does not constitute a specific limitation on the electronic device 100. The electronic device 100 may include components more or fewer than those shown in the figure, or some components may be combined, or some components may be split, or there may be a different component arrangement. The components shown in the figure may be implemented by hardware, software, or a combination of software and hardware.

[0227] Methods or algorithm steps described in combination with the content disclosed in embodiments of this application may be implemented by hardware, or may be implemented by a processor by executing a software instruction. The software instruction may include a corresponding software module. The software module may be stored in a RAM, a flash memory, a ROM,

an erasable programmable read-only memory (Erasable Programmable ROM, EPROM), an electrically erasable programmable read-only memory (Electrically EPROM, EEPROM), a register, a hard disk, a removable hard disk, a compact disc read-only memory (CD-ROM), or any other form of storage medium well-known in the art. For example, a storage medium is coupled to a processor, so that the processor can read information from the storage medium and write information into the storage medium. Certainly, the storage medium may alternatively be a component of the processor. The processor and the storage medium may be disposed in an ASIC. In addition, the ASIC may be located in a transceiver or a relay device. Certainly, the processor and the storage medium may alternatively exist in a wireless access network device or user equipment as discrete components.

[0228] A person skilled in the art should be aware that in the foregoing one or more examples, functions described in embodiments of this application may be implemented by hardware, software, firmware, or any combination thereof. When the functions are implemented by software, the foregoing functions may be stored in a computer-readable medium or transmitted as one or more instructions or code in a computer-readable medium. The computer-readable medium includes a computer storage medium and a communication medium, where the communication medium includes any medium that enables a computer program to be transmitted from one place to another. The storage medium may be any available medium accessible to a general-purpose or a dedicated computer.

[0229] In the foregoing specific implementations, the objectives, the technical solutions, and the beneficial effects of embodiments of this application are further described in detail. It should be understood that the foregoing descriptions are merely specific implementations of embodiments of this application, but are not intended to limit the protection scope of embodiments of this application. Any modification, equivalent replacement, or improvement made based on the technical solutions of embodiments of this application shall fall within the protection scope of embodiments of this application.

Claims

1. A partition refresh method of a display, wherein the display comprises a display circuit, a first gate on array GOA circuit, and a second GOA circuit, the display circuit comprises a plurality of pixel units, the first GOA circuit comprises M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit comprises cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2; and
the method comprises:

   at a moment h, controlling an initial first GOA unit to output the data holding signal, wherein the data holding signal lasts for X row scanning times, and X>N; and
   at a moment k, controlling an initial second GOA unit to output the data writing control signal, wherein the moment k is later than a moment h+N*H and earlier than a moment h+X*H, and H indicates one row scanning time.

2. The method according to claim 1, wherein controlling the initial first GOA unit to output the data holding signal specifically comprises: controlling an i^{th} first GOA unit in the cascaded M*N first GOA units to output the data holding signal at a moment h+(i-1)*Q*H, wherein i is a positive integer, $i \leq M*N$, and Q indicates that the i^{th} first GOA unit outputs the data holding signal Q row scanning times earlier than an $(i+1)^{th}$ first GOA unit.

3. The method according to claim 1 or 2, wherein controlling the initial first GOA unit to output the data holding signal specifically comprises: inputting a start vertical STV signal to an input end of the initial first GOA unit at a moment h-Q*H, wherein Q indicates that the i^{th} first GOA unit outputs the data holding signal Q row scanning times earlier than the $(i+1)^{th}$ first GOA unit.

4. The method according to any one of claims 1 to 3, wherein a calculation formula for a maximum value X_{max} of X is as follows: $X_{max}=M*Y-(M*N-1)*Q$, Y indicates a pulse width of an enable signal on the enable signal line, and Q indicates that the i^{th} first GOA unit outputs the data holding signal Q row scanning times earlier than the $(i+1)^{th}$ first GOA unit.

5. The method according to any one of claims 1 to 4, wherein controlling the initial second GOA unit to output the data writing control signal specifically comprises: starting, by a j^{th} second GOA unit in the cascaded second GOA units, to output the data writing control signal at a moment k+(j-1)*q, wherein q indicates a time by which the j^{th} second GOA unit outputs the data writing control signal later than a $(j-1)^{th}$ second GOA unit, j is a positive integer, and j is less than or equal to a quantity of the cascaded second GOA units.

6. The method according to any one of claims 1 to 5, wherein controlling the initial second GOA unit to output the data writing control signal specifically comprises: inputting a start vertical STV signal to

an input end of the initial second GOA unit at a moment k-q, wherein q indicates the time by which the j^{th} second GOA unit outputs the data writing control signal later than the $(j-1)^{th}$ second GOA unit.

7. The method according to any one of claims 1 to 6, wherein the VFE signal is a high-level signal, the data holding signal is also a high-level signal, and the method further comprises: controlling a time at which the enable signal on the enable signal line switches from a high level to a low level to be later than a first time, wherein the first time is a time at which the data holding signal output by a last first GOA unit connected to the enable signal line switches from a high level to a low level.

8. A partition refresh method of a display, wherein the display comprises a display circuit, a first gate on array GOA circuit, and a second GOA circuit, the display circuit comprises a plurality of pixel units, the first GOA circuit comprises M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit comprises cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2; and
the method comprises:

determining a time for performing data writing into a pixel unit in a first screen area; and
when performing data writing into the pixel unit in the first screen area, performing first bias processing on a reset voltage of the pixel unit in the first screen area, wherein a reset voltage after the first bias processing is a reset voltage corresponding to a first reference luminance at a first refresh rate during data writing; and
the first reference luminance is less than a luminance corresponding to the reset voltage of the pixel unit in the first screen area at the first refresh rate before the first bias processing.

9. The method according to claim 8, wherein the first reference luminance is specifically a luminance corresponding to a first reset voltage at a second refresh rate during data writing, the first reset voltage is a reset voltage of a pixel unit in a second screen area during data writing into the second screen area under refresh at the second refresh rate, and the second refresh rate is higher than the first refresh rate.

10. The method according to claim 9, further comprising: obtaining the first reset voltage through measurement.

11. The method according to claim 9 or 10, wherein the second screen area is a screen area with a highest refresh rate.

12. The method according to any one of claims 8 to 11, further comprising: searching a first mapping table for a luminance corresponding to the first reset voltage, and determining the found luminance as the first reference luminance; and searching a second mapping table for a reset voltage corresponding to the first reference luminance, and determining the found reset voltage as the reset voltage after the first bias processing, wherein
the first mapping table is used to record a correspondence between a reset voltage and a luminance during data writing at the second refresh rate, and the second mapping table is used to record a correspondence between a reset voltage and a luminance during data writing at the first refresh rate.

13. A partition refresh method of a display, wherein the display comprises a display circuit, a first gate on array GOA circuit, and a second GOA circuit, the display circuit comprises a plurality of pixel units, the first GOA circuit comprises M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit comprises cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2; and
the method comprises:

determining a time for skipping performing data writing into a pixel unit in a third screen area, wherein a refresh rate of the third screen area is a third refresh rate; and
when skipping performing data writing into the pixel unit in the third screen area, performing second bias processing on a reset voltage of the pixel unit in the third screen area, wherein a reset voltage after the second bias processing is a reset voltage corresponding to a second reference luminance at the third refresh rate during data holding; and
the second reference luminance is a luminance corresponding to a second reset voltage at the third refresh rate during data writing, and the second reset voltage is a reset voltage during data writing into the third screen area at the third refresh rate.

14. The method according to claim 13, further compris-

ing: obtaining the second reset voltage through measurement.

15. The method according to claim 13 or 14, further comprising: determining a time for performing data writing into the pixel unit in the third screen area.

16. The method according to any one of claims 13 to 15, further comprising:

searching a third mapping table for a luminance corresponding to the second reset voltage, and determining the found luminance as the second reference luminance; and searching a fourth mapping table for a reset voltage corresponding to the second reference luminance, and determining the found reset voltage as the reset voltage after the second bias processing, wherein

the third mapping table is used to record a correspondence between a reset voltage and a luminance during data writing at the third refresh rate, and the fourth mapping table is used to record a correspondence between a reset voltage and a luminance during data holding at the third refresh rate.

17. The method according to any one of claims 13 to 16, wherein the third screen area is specifically the first screen area, and the third refresh rate is specifically the first refresh rate; and
before performing the second bias processing, the method further comprises:

determining a time for performing data writing into a pixel unit in the first screen area; and
when performing data writing into the pixel unit in the first screen area, performing first bias processing on a reset voltage of the pixel unit in the first screen area, wherein a reset voltage after the first bias processing is a reset voltage corresponding to a first reference luminance at the first refresh rate during data writing; and
the first reference luminance is specifically a luminance corresponding to a first reset voltage at a second refresh rate during data writing, the first reset voltage is a reset voltage of a pixel unit in a second screen area during data writing into the second screen area under refresh at the second refresh rate, and the second refresh rate is higher than the first refresh rate.

18. The method according to claim 17, further comprising: obtaining the first reset voltage through measurement.

19. The method according to claim 17 or 18, wherein the second screen area is a screen area with a highest refresh rate.

20. The method according to any one of claims 17 to 19, further comprising: searching a first mapping table for a luminance corresponding to the first reset voltage, and determining the found luminance as the first reference luminance; and searching a second mapping table for a reset voltage corresponding to the first reference luminance, and determining the found reset voltage as the reset voltage after the first bias processing, wherein
the first mapping table is used to record a correspondence between a reset voltage and a luminance during data writing at the second refresh rate, and the second mapping table is used to record a correspondence between a reset voltage and a luminance during data writing at the first refresh rate.

21. A partition refresh method of a display, wherein the display comprises a display circuit, a first gate on array GOA circuit, and a second GOA circuit, the display circuit comprises a plurality of pixel units, the first GOA circuit comprises M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit comprises cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2; and
the method comprises:

determining a gray scale of a pixel unit in a first screen area; and
when performing data writing into a first pixel unit in the first screen area, performing third bias processing on a data voltage of the first pixel unit, wherein a data voltage after the third bias processing is a data voltage corresponding to a third reference luminance at a first refresh rate during data writing, and the first pixel unit is a pixel unit whose gray scale is a first gray scale in the first screen area; and
the third reference luminance is a luminance corresponding to a first data voltage at a second refresh rate, the first data voltage is a data voltage during data writing into a second pixel unit at the second refresh rate, the second pixel unit is a pixel unit whose gray scale is the first gray scale in a second screen area, a refresh rate of the second screen area is the second refresh rate, and the second refresh rate is greater than the first refresh rate.

22. The method according to claim 21, further comprising: obtaining the first data voltage through measure-

ment.

23. The method according to claim 21 or 22, further comprising:

searching a fifth mapping table for a luminance corresponding to the first data voltage, and determining the found luminance as the third reference luminance; and searching a sixth mapping table for a data voltage corresponding to the third reference luminance, and determining the found luminance as the data voltage after the third bias processing, wherein
the fifth mapping table is used to record a correspondence between a data voltage and a luminance during data writing at the second refresh rate, and the sixth mapping table is used to record a correspondence between a data voltage and a luminance during data writing at the first refresh rate.

24. A partition refresh method of a display, wherein the display comprises a display circuit, a first gate on array GOA circuit, and a second GOA circuit, the display circuit comprises a plurality of pixel units, the first GOA circuit comprises M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit comprises cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2; and the method comprises:

determining a time for skipping performing data writing into a pixel unit in a fourth screen area, wherein a refresh rate of the fourth screen area is a fourth refresh rate; and
when skipping performing data writing into the pixel unit in the fourth screen area, performing fourth bias processing on a data voltage of a third pixel unit in the fourth screen area, wherein a data voltage after the fourth bias processing is a data voltage corresponding to a fourth reference luminance at the fourth refresh rate during data holding; and
the fourth reference luminance is a luminance corresponding to a second data voltage at the fourth refresh rate during data writing into the fourth screen area, and the second data voltage is a data voltage during data writing into the third pixel unit at the fourth refresh rate.

25. The method according to claim 24, further comprising: obtaining the second data voltage through measurement.

26. The method according to claim 24 or 25, further comprising: determining a time for skipping performing data writing into the fourth screen area.

27. The method according to any one of claims 24 to 26, further comprising: searching a seventh mapping table for a luminance corresponding to the second data voltage, and determining the found luminance as the fourth reference luminance; and searching an eighth mapping table for a data voltage corresponding to the fourth reference luminance, and determining the found data voltage as the data voltage after the fourth bias processing, wherein
the seventh mapping table is used to record a correspondence between a data voltage and a luminance during data writing at the fourth refresh rate, and the eighth mapping table is used to record a correspondence between a data voltage and a luminance during data holding at the fourth refresh rate.

28. The method according to any one of claims 24 to 26, wherein the fourth screen area is specifically a first screen area, and the fourth refresh rate is specifically a first refresh rate; and
before performing the fourth bias, the method further comprises:

determining a gray scale of a pixel unit in the first screen area; and
when performing data writing into a first pixel unit in the first screen area, performing third bias processing on a data voltage of the first pixel unit, wherein a data voltage after the third bias processing is a data voltage corresponding to a third reference luminance at the first refresh rate during data writing, and the first pixel unit is a pixel unit whose gray scale is a first gray scale in the first screen area; and
the third reference luminance is a luminance corresponding to a first data voltage at a second refresh rate, the first data voltage is a data voltage during data writing into a second pixel unit at the second refresh rate, the second pixel unit is a pixel unit whose gray scale is the first gray scale in a second screen area, a refresh rate of the second screen area is the second refresh rate, and the second refresh rate is greater than the first refresh rate.

29. The method according to claim 28, further comprising: obtaining the first data voltage through measurement.

30. The method according to claim 28 or 29, further comprising:

searching a fifth mapping table for a luminance corresponding to the first data voltage, and de-

termining the found luminance as the third reference luminance; and searching a sixth mapping table for a data voltage corresponding to the third reference luminance, and determining the found luminance as the data voltage after the third bias processing, wherein
the fifth mapping table is used to record a correspondence between a data voltage and a luminance during data writing at the second refresh rate, and the sixth mapping table is used to record a correspondence between a data voltage and a luminance during data writing at the first refresh rate.

31. An electronic device, comprising a display, a processor, and a memory, wherein the display is coupled to the processor, and the memory is coupled to the processor;

the display comprises a display circuit, a first gate on array GOA circuit, and a second GOA circuit, the display circuit comprises a plurality of pixel units, the first GOA circuit comprises M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit comprises cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2; and
the memory is configured to store computer program code, the computer program code comprises computer instructions, and when the processor executes the computer instructions, the method according to any one of claims 1 to 30 is performed.

32. A display system, wherein the display system comprises a display and a control circuit;

the display comprises a display circuit, a first gate on array GOA circuit, and a second GOA circuit, the display circuit comprises a plurality of pixel units, the first GOA circuit comprises M*N cascaded first GOA units, the first GOA circuit is connected to M enable signal lines, one enable signal line is connected to N stages of first GOA units, the first GOA unit is configured to output a data holding signal to the pixel unit, the second GOA circuit comprises cascaded second GOA units, the second GOA unit is configured to output a data writing control signal to the pixel unit, M and N are positive integers, and M is greater than or equal to 2; and
the control circuit is configured to invoke computer instructions, so that the method according to any one of claims 1 to 29 is performed.

33. A computer-readable storage medium, comprising instructions, wherein when the instructions are run on an electronic device, the method according to any one of claims 1 to 30 is performed.

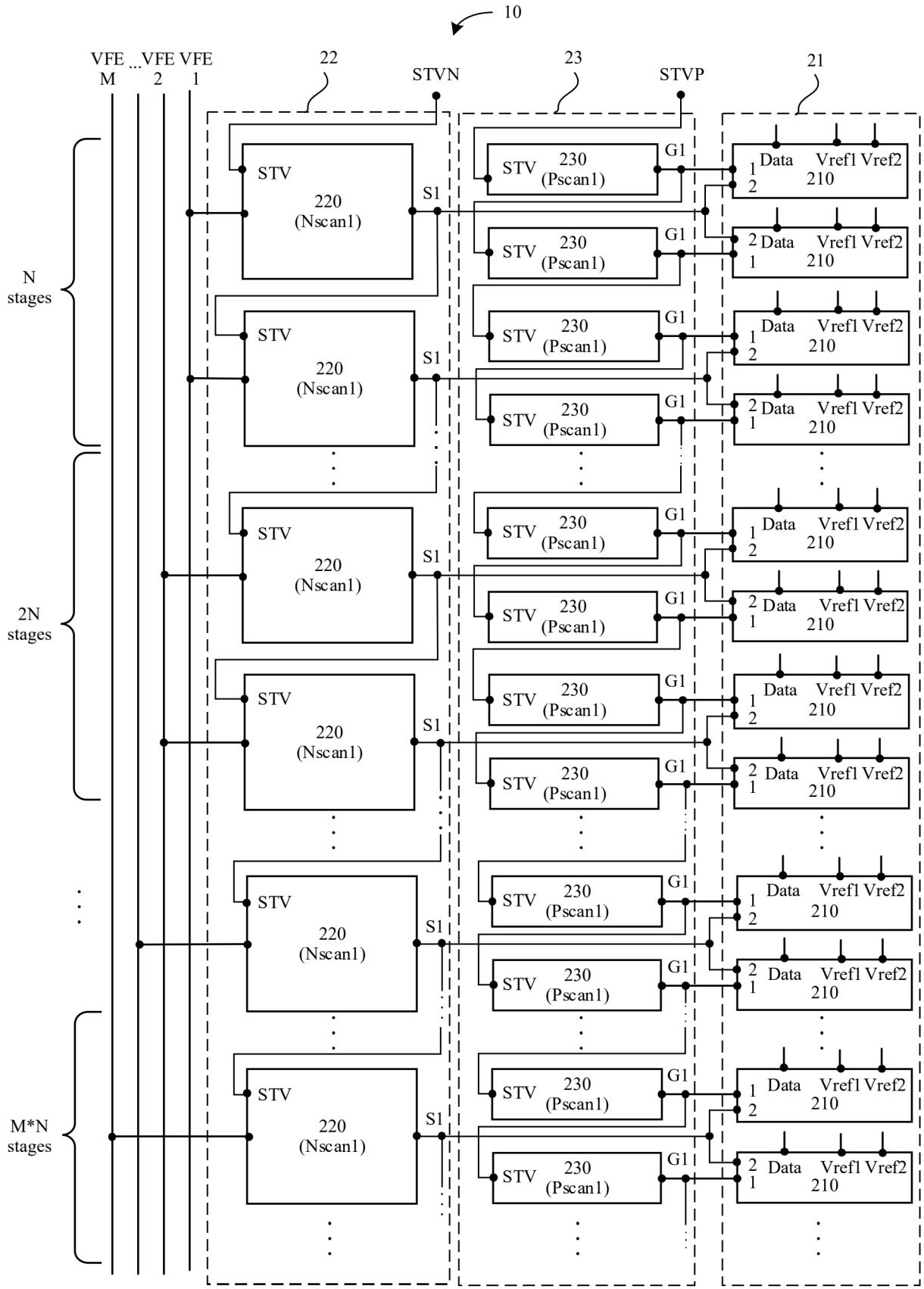

10
VFE M
VFE 2
VFE 1
22
STVN
23
STVP
21
N stages
2N stages
M*N stages
STV
220 (Nscan1)
S1
230 (Pscan1)
G1
Data
Vref1
Vref2
210

FIG. 1

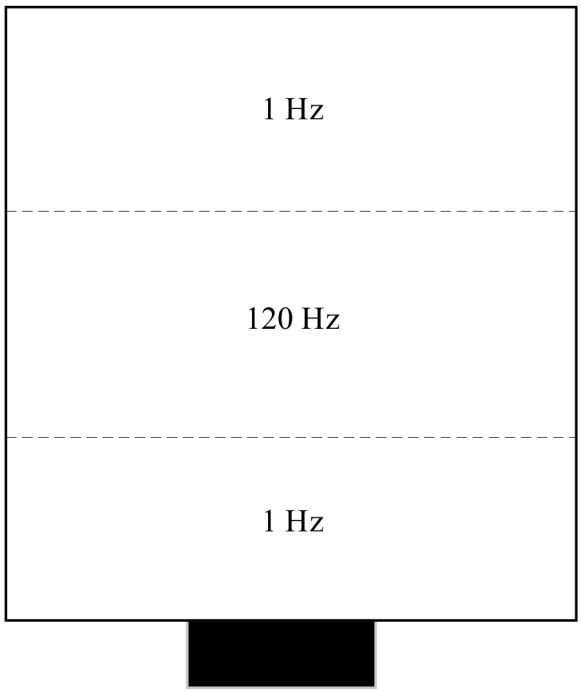

1 Hz
120 Hz
1 Hz

FIG. 2

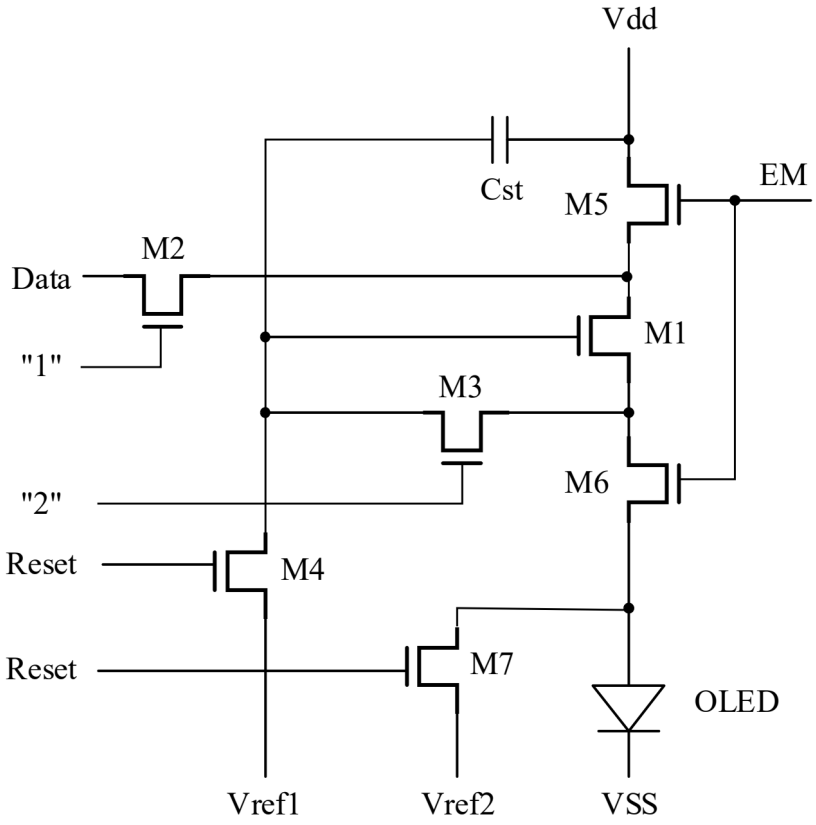

Vdd
Cst
M5
EM
M2
Data
"1"
M1
M3
"2"
M6
Reset
M4
Reset
M7
OLED
Vref1
Vref2
VSS

FIG. 3

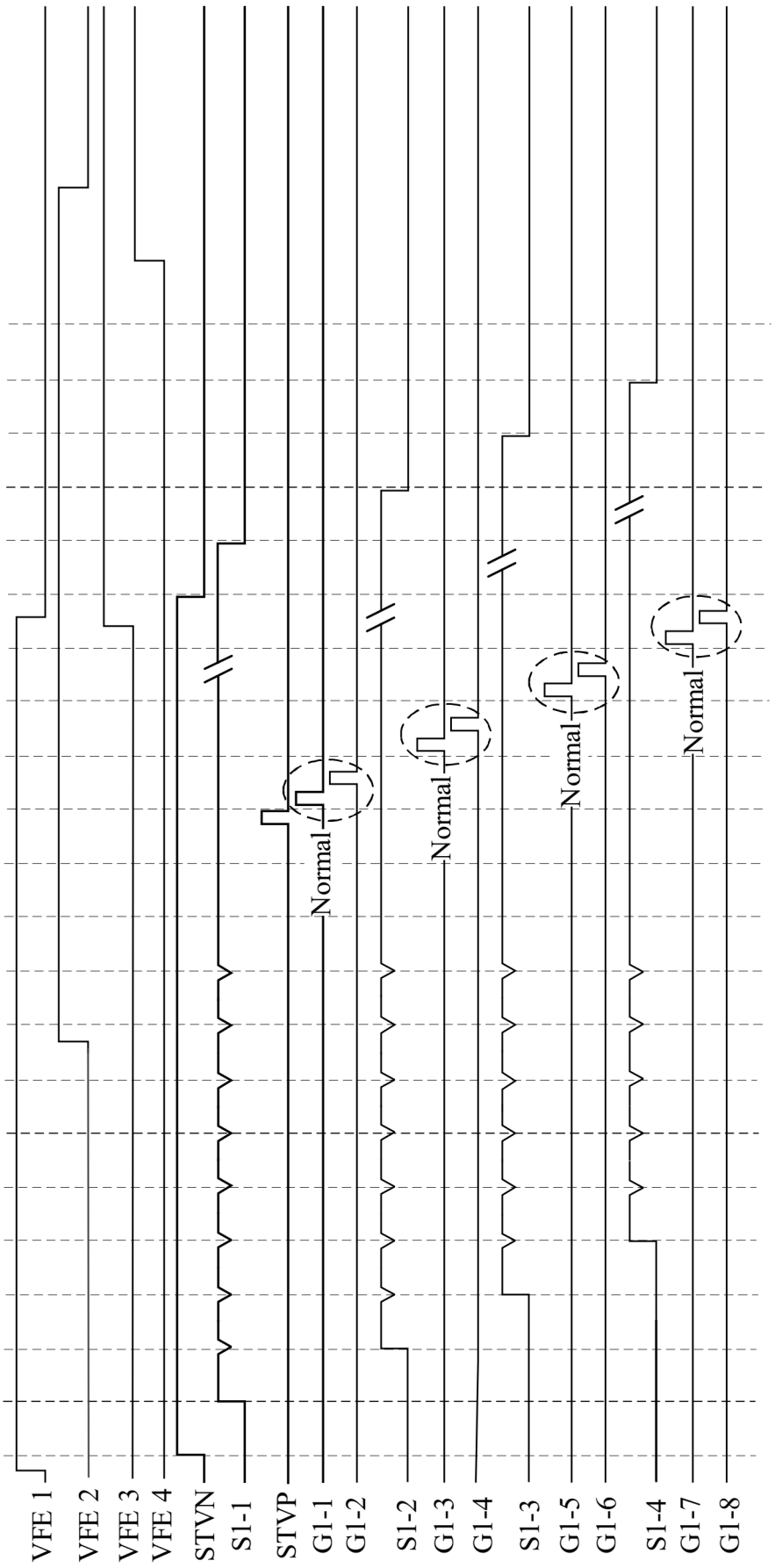

VFE 1
VFE 2
VFE 3
VFE 4
STVN
S1-1
STVP
G1-1
G1-2
S1-2
G1-3
G1-4
S1-3
G1-5
G1-6
S1-4
G1-7
G1-8
Normal
Normal
Normal
Normal

FIG. 4

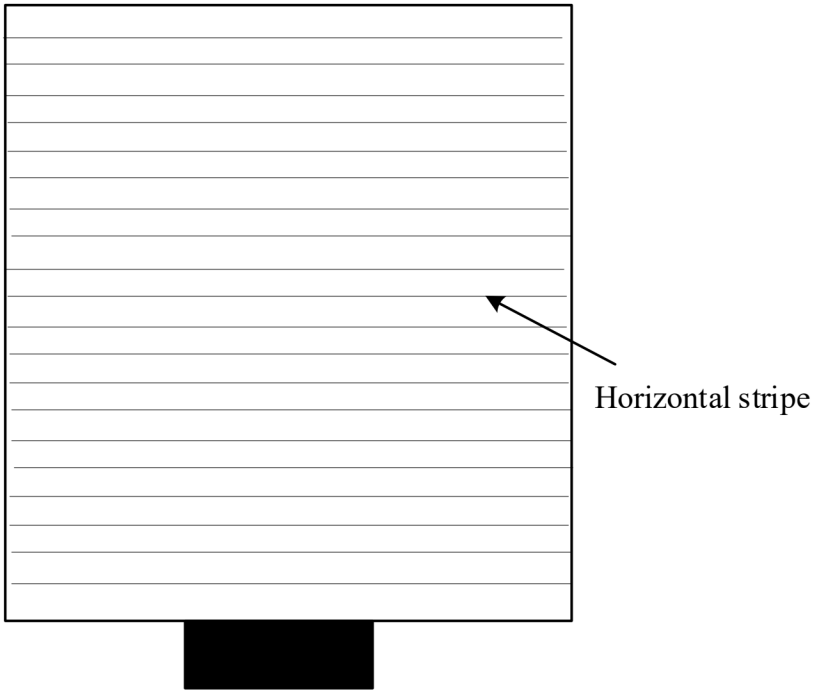


FIG. 5

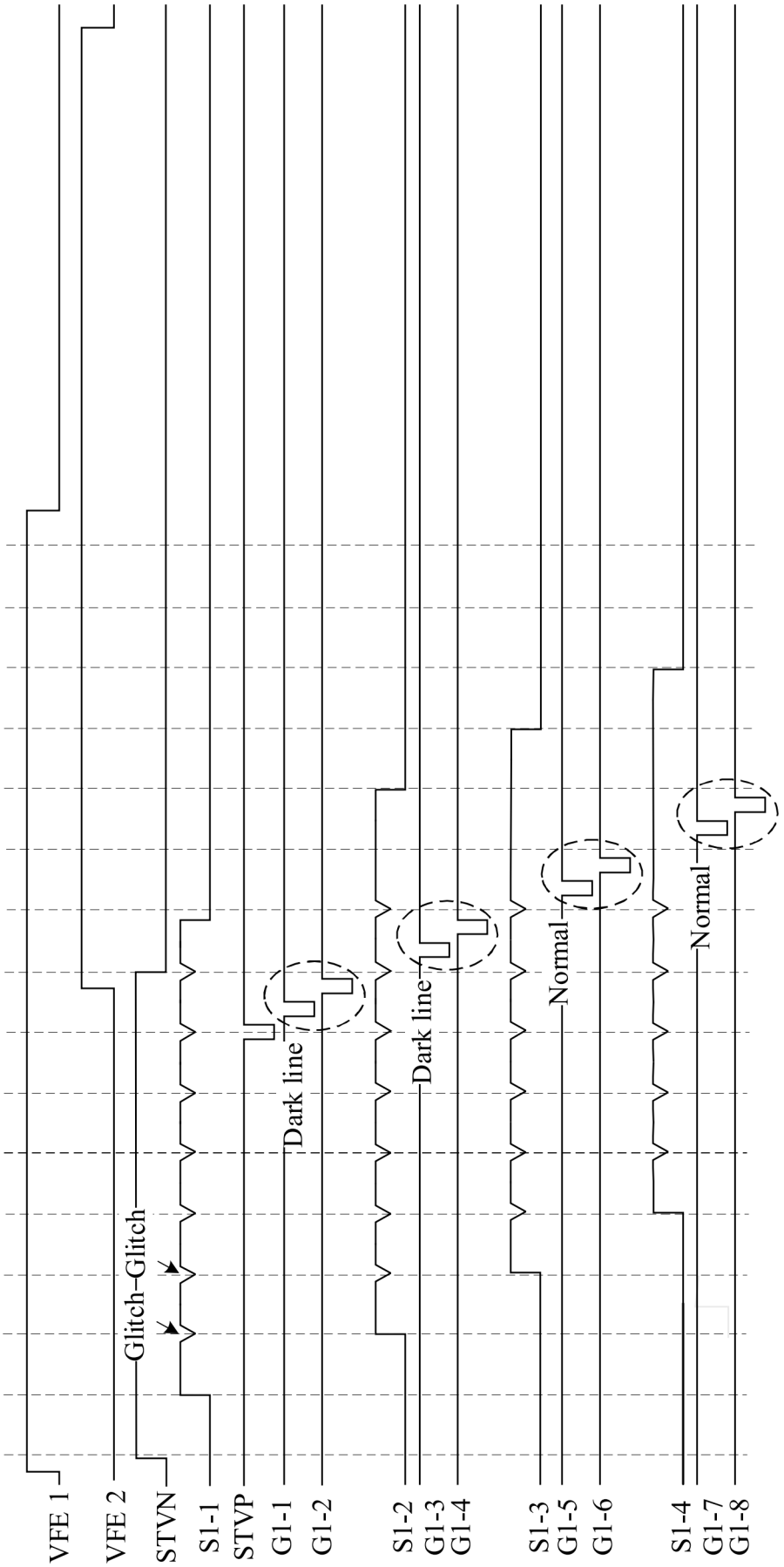

VFE 1
VFE 2
STVN
S1-1
STVP
G1-1
G1-2
S1-2
G1-3
G1-4
S1-3
G1-5
G1-6
S1-4
G1-7
G1-8
Glitch
Glitch
Dark line
Dark line
Normal
Normal

FIG. 6

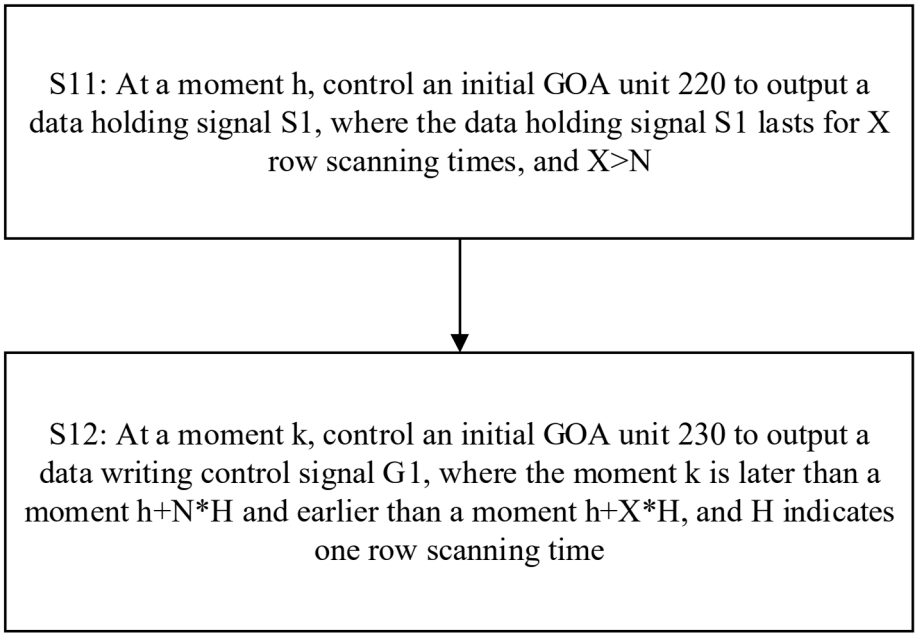

S11: At a moment h, control an initial GOA unit 220 to output a data holding signal S1, where the data holding signal S1 lasts for X row scanning times, and X>N
S12: At a moment k, control an initial GOA unit 230 to output a data writing control signal G1, where the moment k is later than a moment h+N*H and earlier than a moment h+X*H, and H indicates one row scanning time

FIG. 7

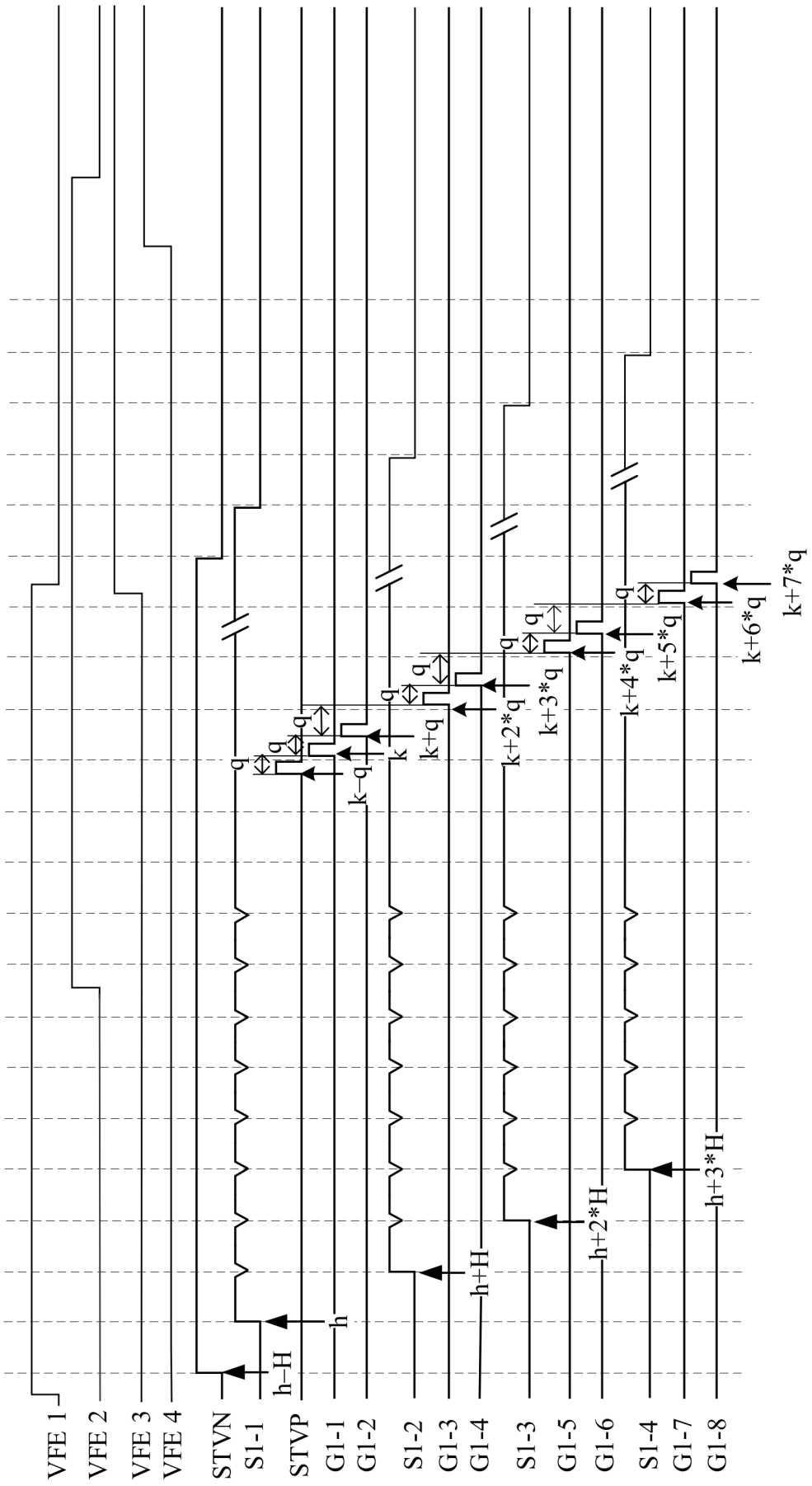

VFE 1
VFE 2
VFE 3
VFE 4
STVN
S1-1
STVP
G1-1
G1-2
S1-2
G1-3
G1-4
S1-3
G1-5
G1-6
S1-4
G1-7
G1-8
h–H
h
k–q
k
k+q
h+H
k+2*q
k+3*q
h+2*H
k+4*q
k+5*q
h+3*H
k+6*q
k+7*q
q

FIG. 8

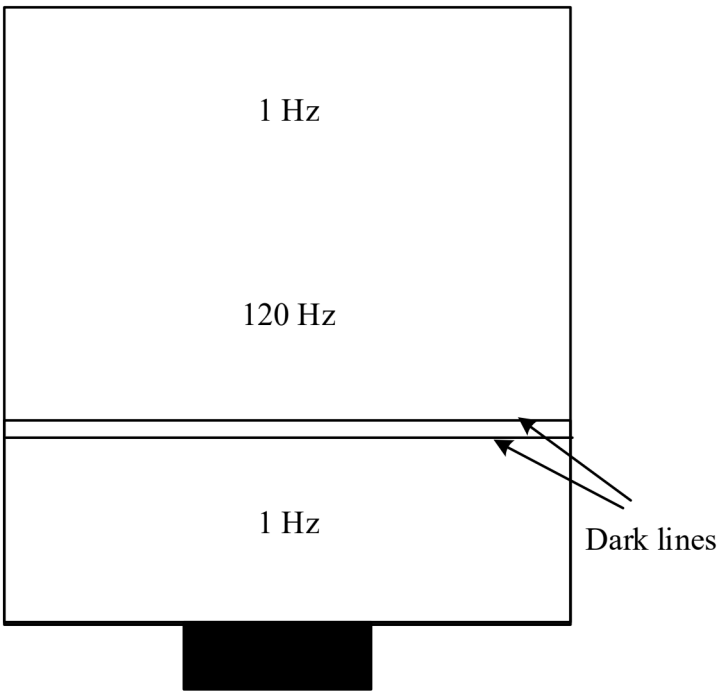
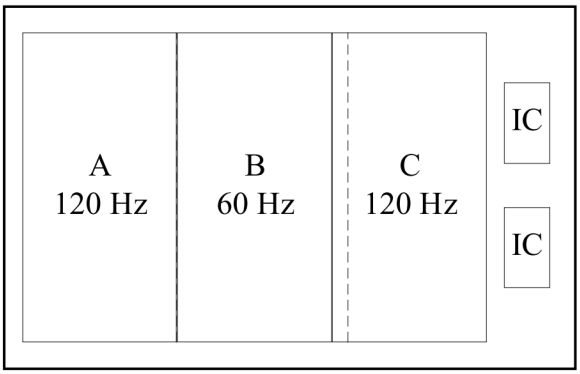
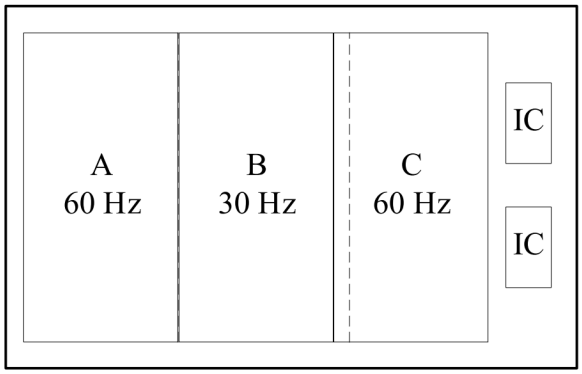


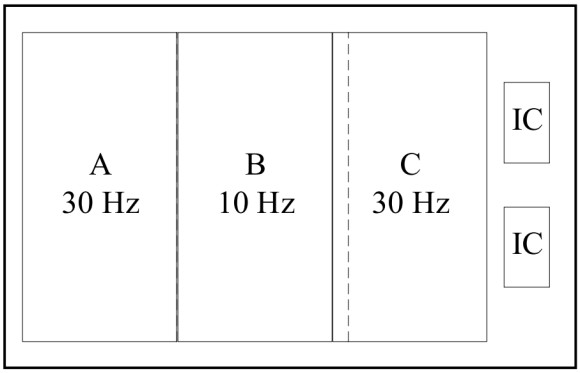
FIG. 9



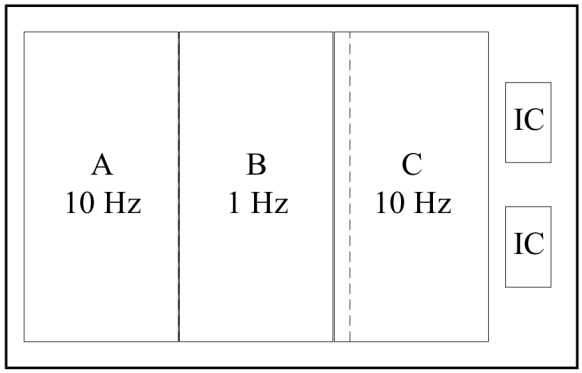
Frequency	Luminance (nit)
120 (A)	2.12
60 (B)	2.51
120 (C)	2.11



Frequency	Luminance (nit)
60 (A)	2.58
30 (B)	2.66
60 (C)	2.56



Frequency	Luminance (nit)
30 (A)	2.65
10 (B)	2.88
30 (C)	2.67



Frequency	Luminance (nit)
10 (A)	2.89
1 (B)	3.01
10 (C)	2.85

FIG. 10

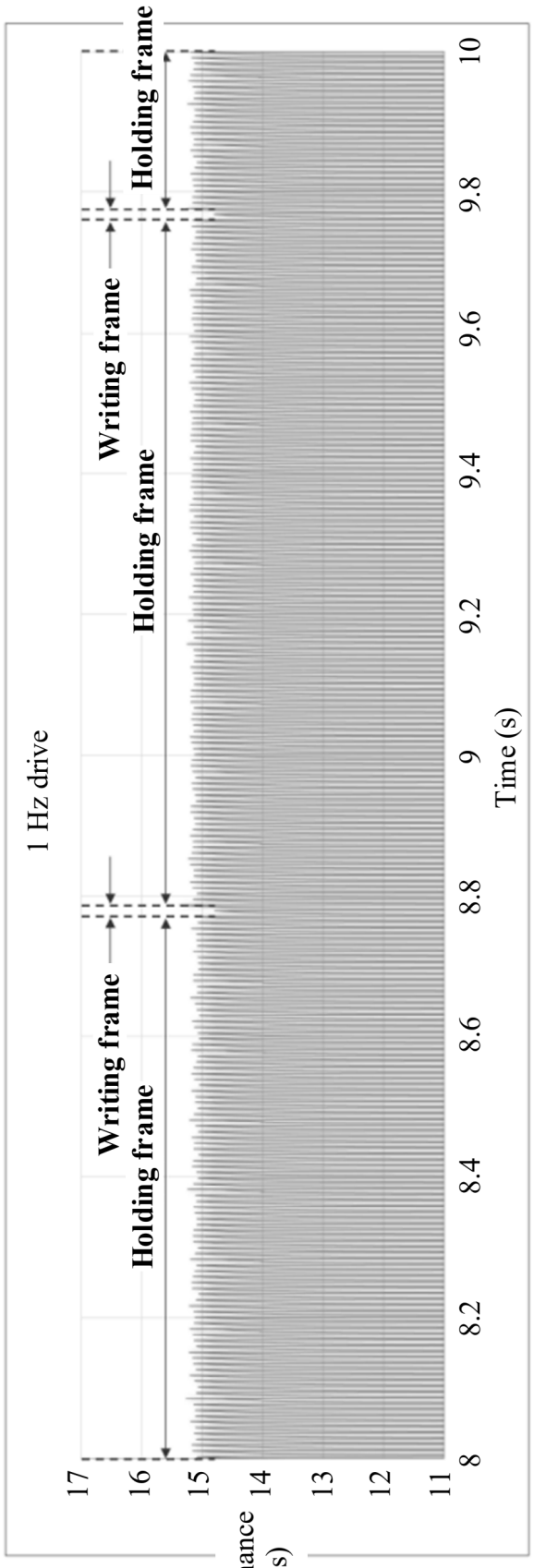

1 Hz drive
Writing frame
Holding frame
Writing frame
Holding frame
Holding frame
Luminance (nits)
17
16
15
14
13
12
11
8
8.2
8.4
8.6
8.8
9
9.2
9.4
9.6
9.8
10
Time (s)

FIG. 11

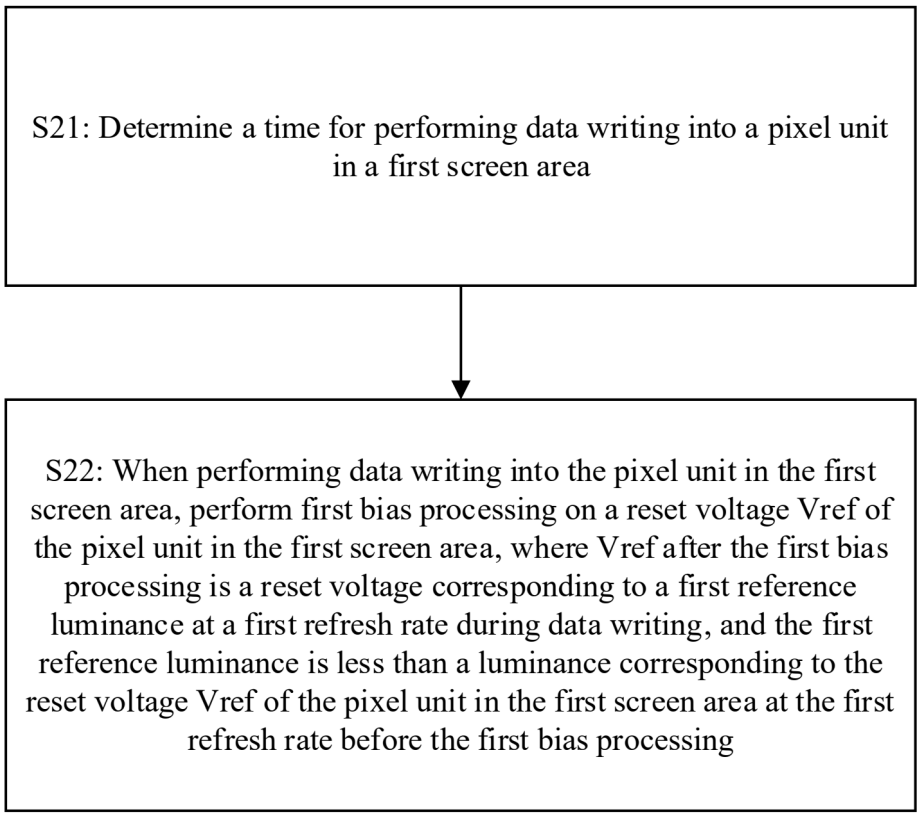

S21: Determine a time for performing data writing into a pixel unit in a first screen area
S22: When performing data writing into the pixel unit in the first screen area, perform first bias processing on a reset voltage Vref of the pixel unit in the first screen area, where Vref after the first bias processing is a reset voltage corresponding to a first reference luminance at a first refresh rate during data writing, and the first reference luminance is less than a luminance corresponding to the reset voltage Vref of the pixel unit in the first screen area at the first refresh rate before the first bias processing

FIG. 12

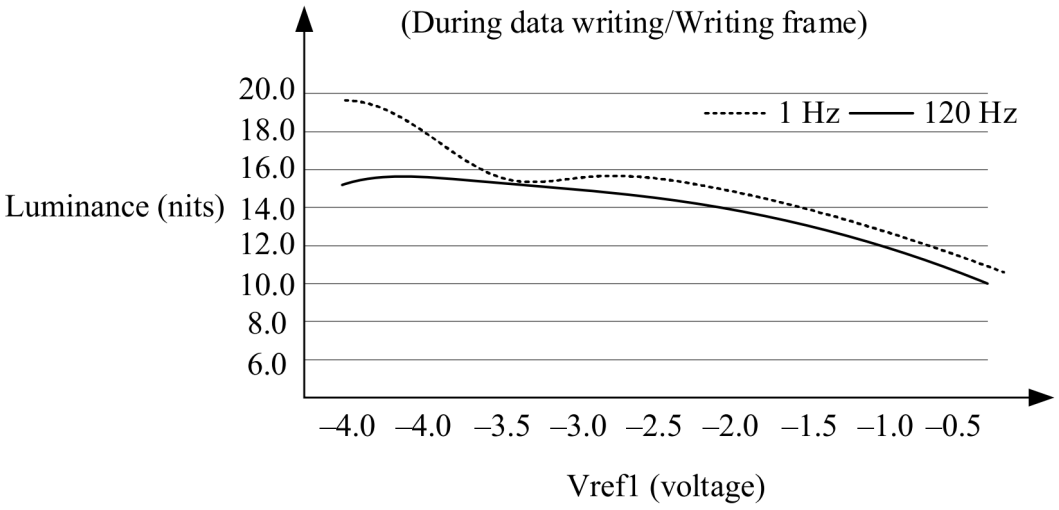

(During data writing/Writing frame)
1 Hz
120 Hz
Luminance (nits)
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
–4.0 –4.0 –3.5 –3.0 –2.5 –2.0 –1.5 –1.0 –0.5
Vref1 (voltage)

FIG. 13

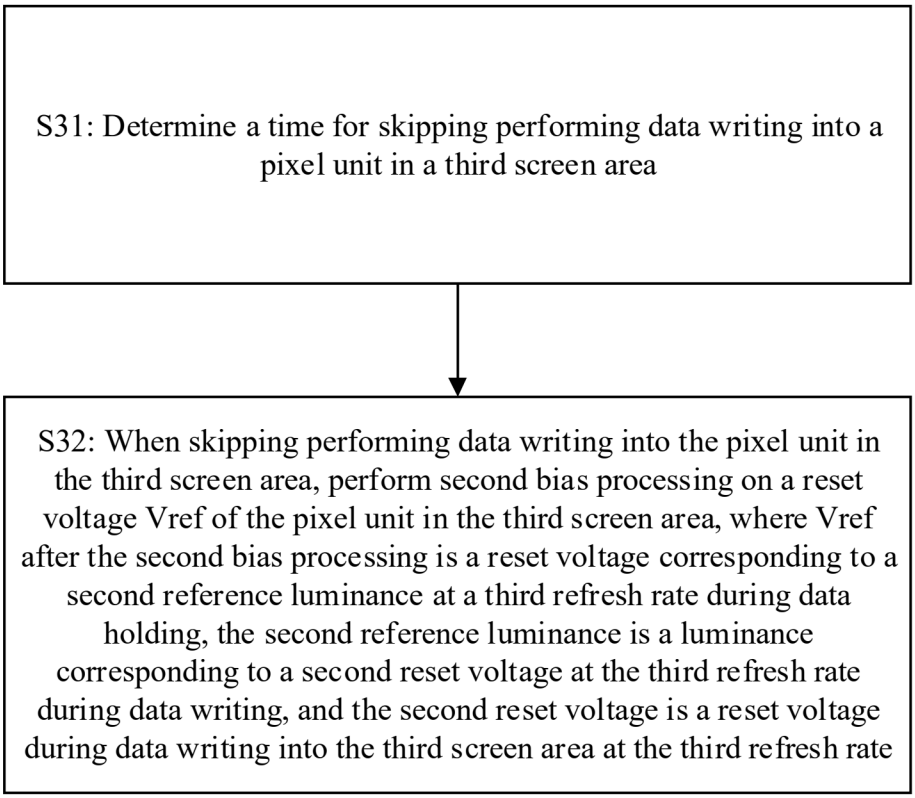

S31: Determine a time for skipping performing data writing into a pixel unit in a third screen area
S32: When skipping performing data writing into the pixel unit in the third screen area, perform second bias processing on a reset voltage Vref of the pixel unit in the third screen area, where Vref after the second bias processing is a reset voltage corresponding to a second reference luminance at a third refresh rate during data holding, the second reference luminance is a luminance corresponding to a second reset voltage at the third refresh rate during data writing, and the second reset voltage is a reset voltage during data writing into the third screen area at the third refresh rate

FIG. 14

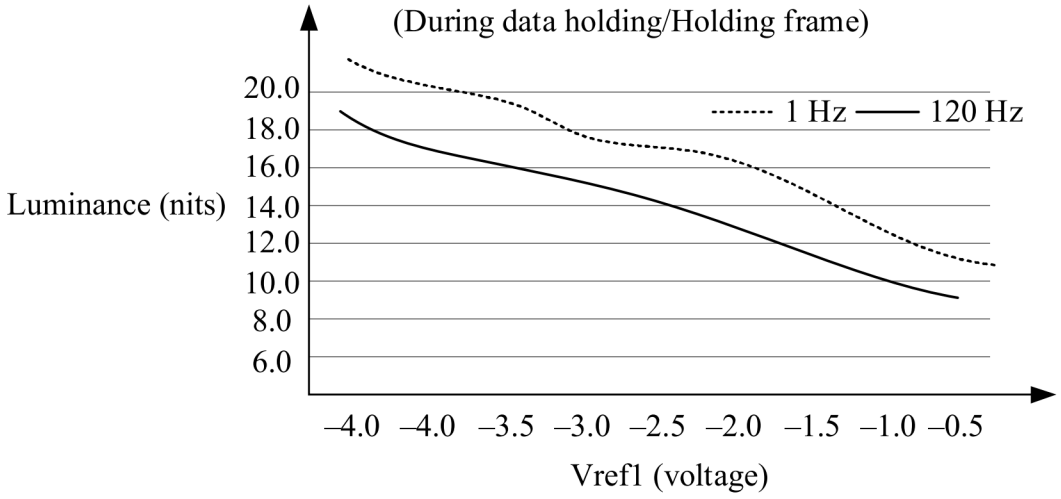

(During data holding/Holding frame)
Luminance (nits)
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
1 Hz
120 Hz
–4.0 –4.0 –3.5 –3.0 –2.5 –2.0 –1.5 –1.0 –0.5
Vref1 (voltage)

FIG. 15

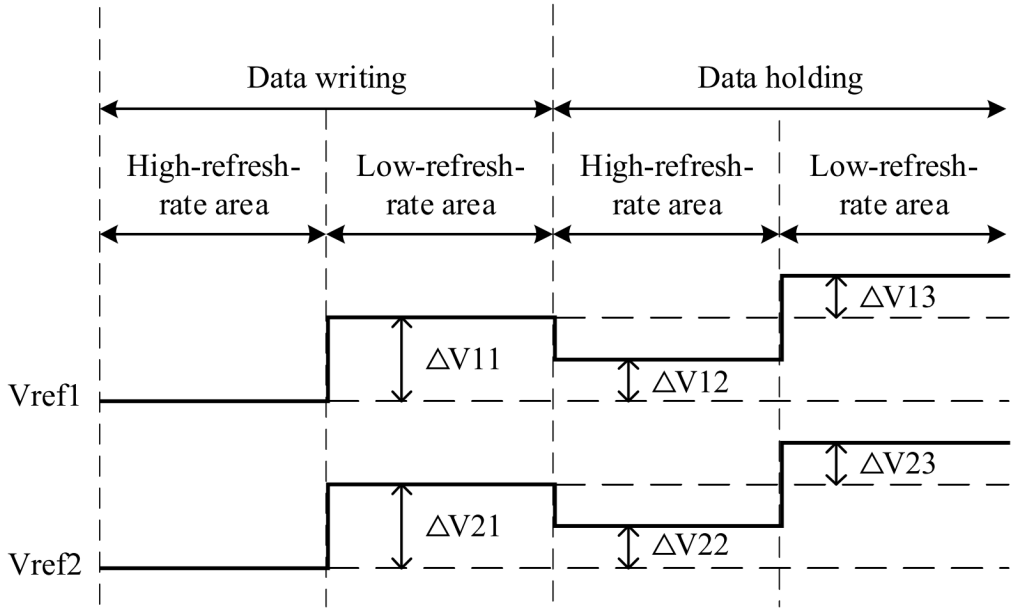

Data writing
Data holding
High-refresh-rate area
Low-refresh-rate area
High-refresh-rate area
Low-refresh-rate area
ΔV13
ΔV11
ΔV12
Vref1
ΔV23
ΔV21
ΔV22
Vref2

FIG. 16

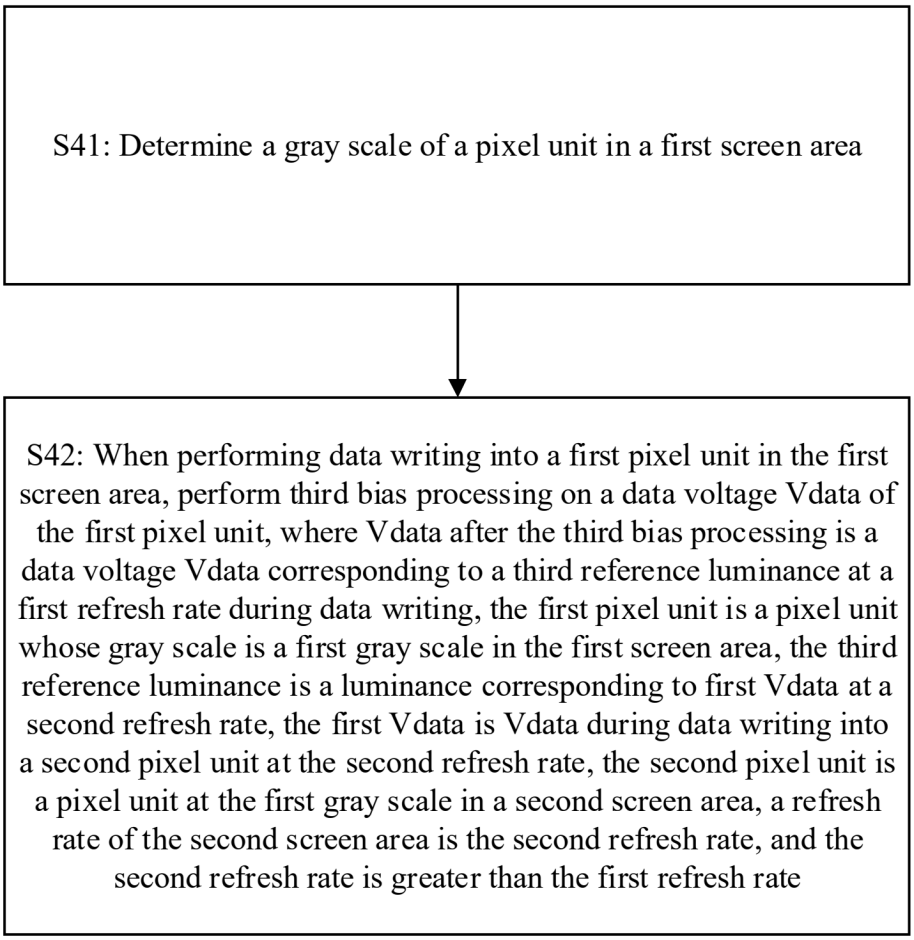

S41: Determine a gray scale of a pixel unit in a first screen area
S42: When performing data writing into a first pixel unit in the first screen area, perform third bias processing on a data voltage Vdata of the first pixel unit, where Vdata after the third bias processing is a data voltage Vdata corresponding to a third reference luminance at a first refresh rate during data writing, the first pixel unit is a pixel unit whose gray scale is a first gray scale in the first screen area, the third reference luminance is a luminance corresponding to first Vdata at a second refresh rate, the first Vdata is Vdata during data writing into a second pixel unit at the second refresh rate, the second pixel unit is a pixel unit at the first gray scale in a second screen area, a refresh rate of the second screen area is the second refresh rate, and the second refresh rate is greater than the first refresh rate

FIG. 17

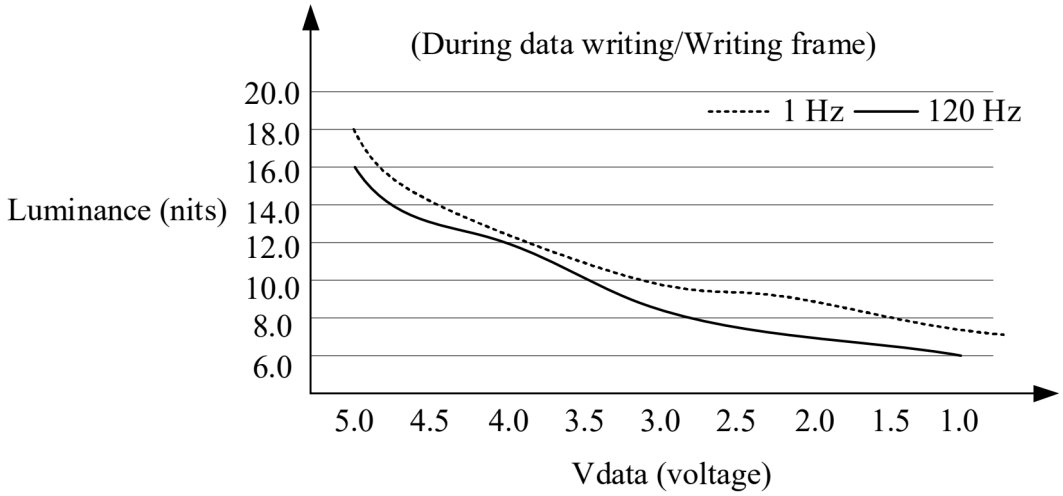

(During data writing/Writing frame)
1 Hz
120 Hz
Luminance (nits)
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
Vdata (voltage)

FIG. 18

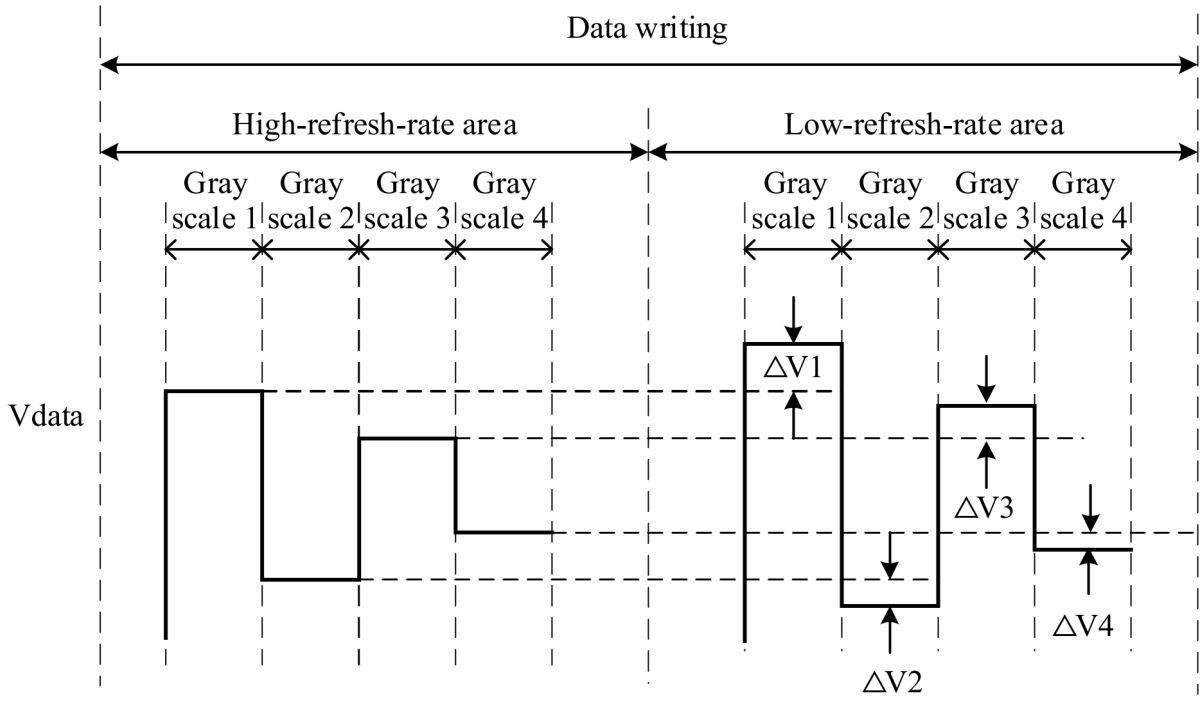

Data writing
High-refresh-rate area
Low-refresh-rate area
Gray scale 1
Gray scale 2
Gray scale 3
Gray scale 4
Gray scale 1
Gray scale 2
Gray scale 3
Gray scale 4
Vdata
ΔV1
ΔV2
ΔV3
ΔV4

FIG. 19

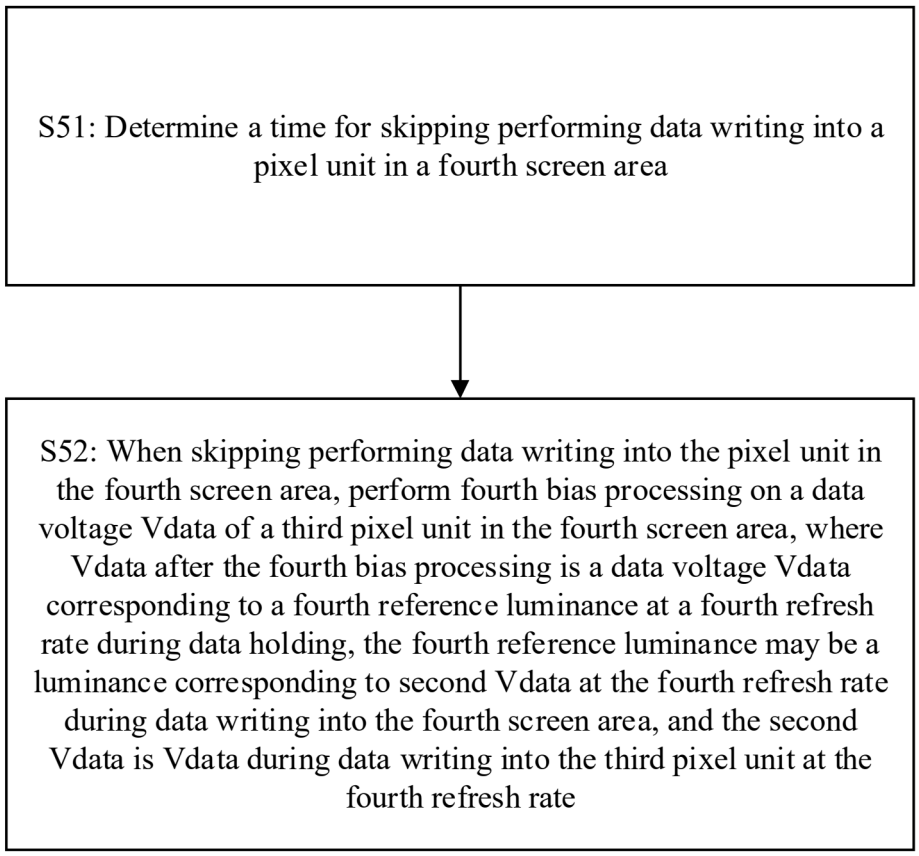

S51: Determine a time for skipping performing data writing into a pixel unit in a fourth screen area
S52: When skipping performing data writing into the pixel unit in the fourth screen area, perform fourth bias processing on a data voltage Vdata of a third pixel unit in the fourth screen area, where Vdata after the fourth bias processing is a data voltage Vdata corresponding to a fourth reference luminance at a fourth refresh rate during data holding, the fourth reference luminance may be a luminance corresponding to second Vdata at the fourth refresh rate during data writing into the fourth screen area, and the second Vdata is Vdata during data writing into the third pixel unit at the fourth refresh rate

FIG. 20

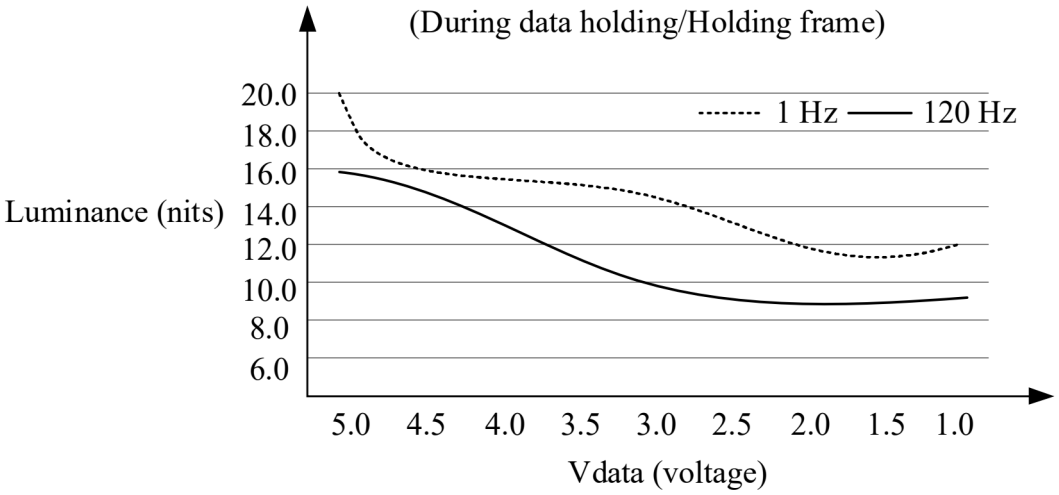

(During data holding/Holding frame)
1 Hz
120 Hz
Luminance (nits)
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
Vdata (voltage)

FIG. 21

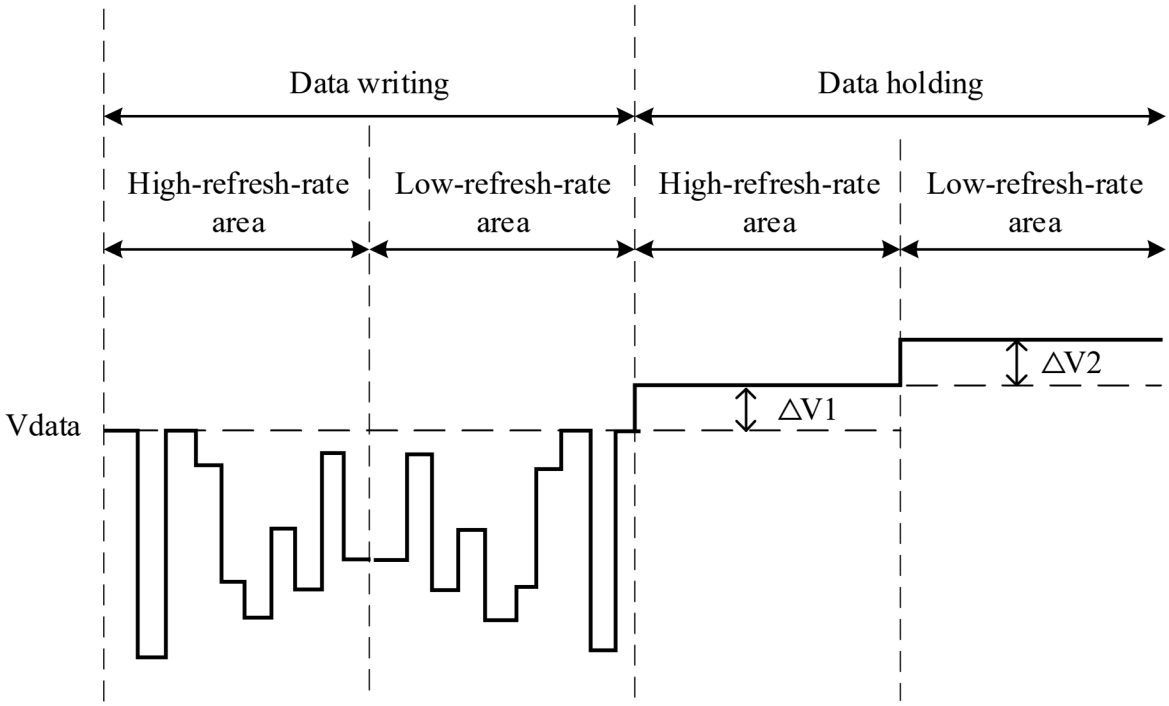

Data writing
Data holding
High-refresh-rate area
Low-refresh-rate area
High-refresh-rate area
Low-refresh-rate area
Vdata
△V1
△V2

FIG. 22

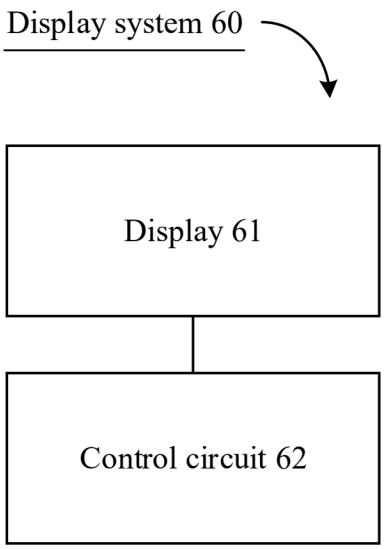

Display system 60
Display 61
Control circuit 62

FIG. 23

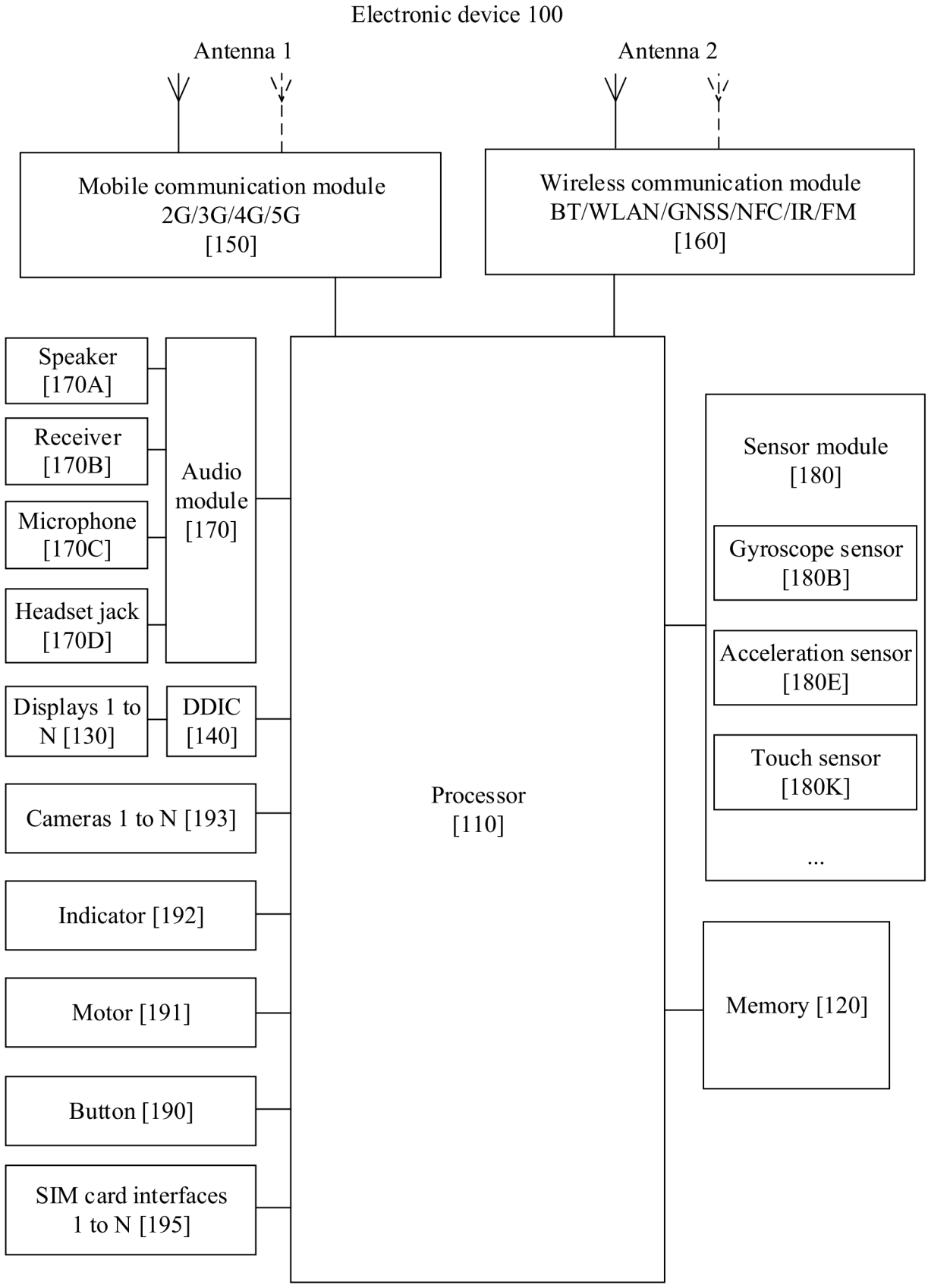

Electronic device 100
Antenna 1
Antenna 2
Mobile communication module
2G/3G/4G/5G
[150]
Wireless communication module
BT/WLAN/GNSS/NFC/IR/FM
[160]
Speaker
[170A]
Receiver
[170B]
Microphone
[170C]
Headset jack
[170D]
Audio
module
[170]
Displays 1 to
N [130]
DDIC
[140]
Cameras 1 to N [193]
Indicator [192]
Motor [191]
Button [190]
SIM card interfaces
1 to N [195]
Processor
[110]
Sensor module
[180]
Gyroscope sensor
[180B]
Acceleration sensor
[180E]
Touch sensor
[180K]
...
Memory [120]

FIG. 24

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2024/130762

A. CLASSIFICATION OF SUBJECT MATTER

G09G 5/393(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC:G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS, CNTXT, CNKI, VEN, USTXT, EPTXT, WOTXT: 华为技术有限公司, 显示装置, 显示器, 分区, 不同区域, 刷新, 第一GOA, 第二GOA, 使能信号, DE信号, 数据保持信号, 行扫描信号, 行扫描时间, 复位电压, 偏置, 毛刺, 横纹, 亮度差, 闪烁, display device, partition, different area, refresh, first GOA, second GOA, enable signal, DE signal, data retention signal, row scan signal, row scan time, reset voltage, bias, burr, horizontal stripe, brightness difference, flicker

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 115775547 A (BOE TECHNOLOGY GROUP CO., LTD. et al.) 10 March 2023 (2023-03-10) description, paragraphs 0059-0099, and figures 4-9	1-33
A	CN 116343666 A (BOE TECHNOLOGY GROUP CO., LTD. et al.) 27 June 2023 (2023-06-27) entire document	1-33
A	CN 113823207 A (HUAWEI TECHNOLOGIES CO., LTD.) 21 December 2021 (2021-12-21) entire document	1-33
A	CN 115311996 A (BOE TECHNOLOGY GROUP CO., LTD.) 08 November 2022 (2022-11-08) entire document	1-33
A	CN 115312004 A (XIAMEN TIANMA DISPLAY TECHNOLOGY CO., LTD.) 08 November 2022 (2022-11-08) entire document	1-33

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
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"D" document cited by the applicant in the international application
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 January 2025	**31 January 2025**
Name and mailing address of the ISA/CN **China National Intellectual Property Administration (ISA/CN)** **China No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing 100088**	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 2022)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2024/130762

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
CN 115775547 A	10 March 2023	None	
CN 116343666 A	27 June 2023	None	
CN 113823207 A	21 December 2021	None	
CN 115311996 A	08 November 2022	None	
CN 115312004 A	08 November 2022	None	

Form PCT/ISA/210 (patent family annex) (July 2022)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- CN 202311554390 **[0001]**