



(11) **EP 4 766 067 A8**

(12) **CORRECTED EUROPEAN PATENT APPLICATION**

(15) Correction information:
Corrected version no 1 (W1 A2)
Corrections, see
Bibliography INID code(s) 71

(51) International Patent Classification (IPC):
H10B 41/30 (2023.01) **H10D 30/68** (2025.01)
H10D 64/01 (2025.01) **H10B 41/10** (2023.01)
H10D 30/01 (2025.01)

(48) Corrigendum issued on:
21.10.2026 Bulletin 2026/43

(52) Cooperative Patent Classification (CPC):
H10B 41/30; H10B 41/10; H10D 30/0411;
H10D 30/6891; H10D 30/6892; H10D 30/6894;
H10D 64/035

(43) Date of publication:
24.06.2026 Bulletin 2026/26

(21) Application number: **25220708.9**

(22) Date of filing: **04.12.2025**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HR HU IE IS IT LI LT LU LV MC ME MK MT NL
NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA
Designated Validation States:
GE KH LA MA MD TN

- **GigaDevice Semiconductor Inc.**
Haidian, Beijing 100094 (CN)
- **Suzhou Freethink Information Technology Co.,**
Ltd.
Jiangsu 215000 (CN)

(30) Priority: **19.12.2024 CN 202411887429**

(71) Applicants:

- **GigaDevice Semiconductor (Shanghai) Inc.**
Shanghai 201210 (CN)
- **GIGADEVICE SEMICONDUCTOR (HEFEI) INC.**
Hefei Anhui 230031 (CN)
- **GIGADEVICE SEMICONDUCTOR (XIAN) INC.**
Xi'an Shaanxi 710065 (CN)

(72) Inventors:

- **XU, Jing**
No.505 Zhangjiang Road, Shanghai, 201210 (CN)
- **QIAN, Meng**
No.505 Zhangjiang Road, Shanghai, 201210 (CN)
- **XU, Yisheng**
No.505 Zhangjiang Road, Shanghai, 201210 (CN)

(74) Representative: **Herrero & Asociados, S.L.**
Edificio Aqua - Calle Agustín de Foxá, 4-10, 2^oA
28036 Madrid (ES)

(54) **METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, AND MEMORY DEVICE**

(57) A method for manufacturing a semiconductor device (10), a semiconductor device (10), and a memory device (1) are provided. The method includes forming (11, 21) shallow trench isolation structures (400) in a substrate (100), where first trenches (B) are defined between adjacent protruding portions of the shallow trench isolation structures (400); forming (12, 22) floating gates (500) in first trenches (B) and performing a first etching on a part of the protruding portions to form second trenches (C) between the adjacent floating gates (500); performing (13, 23) a narrowing process on the floating gates (500); performing (14, 24) a second etching on a remaining part of the protruding portions to widen the second trenches (C); and forming (15, 26) a control gate (600) partially filled in the second trenches (C).

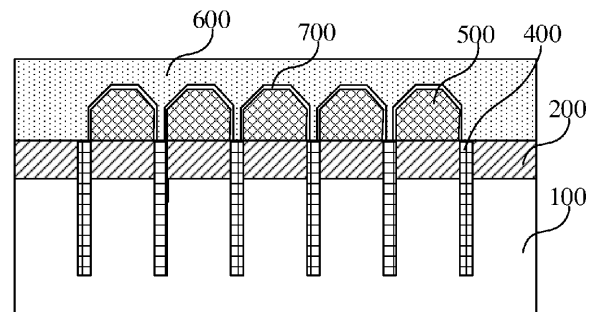


FIG. 14