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(71) Applicant: **Yas Co., Ltd.**
Paju-si, Gyeonggi-do 10857 (KR)

(72) Inventor: **KIM, Bumsik**
Paju-si, Gyeonggi-do 10857 (KR)

(74) Representative: **Epping - Hermann - Fischer**
Patentanwalts-gesellschaft mbH
Schloßschmidstraße 5
80639 München (DE)

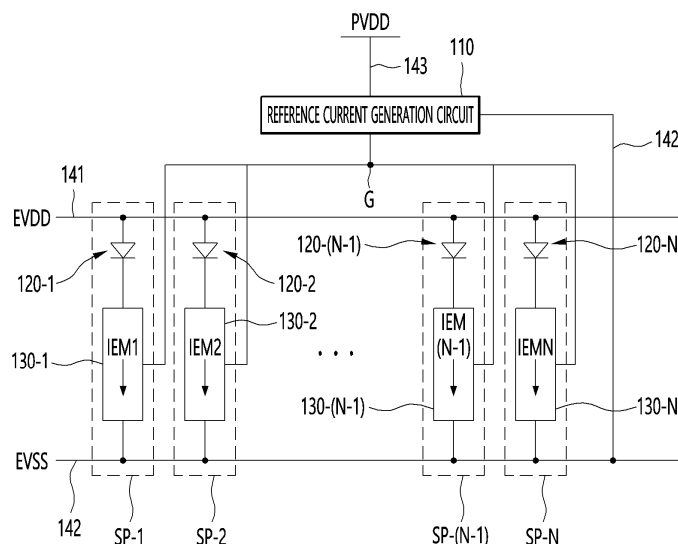
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(54) **DISPLAY DEVICE**

(57) The display device may include a reference current generation circuit and a plurality of light-emitting circuits. The reference current generation circuit may include a constant current source that generates a reference current. The plurality of light-emitting circuits may be provided in a plurality of subpixels and may be electrically connected to the reference current generation

circuit. The plurality of light-emitting circuits may each generate a light-emitting current by using the reference current to emit light from a light-emitting element, and may control an emission time of the light-emitting element by using digital data and a program signal. The reference current and the light-emitting current may be constant currents.

FIG. 2



Description

[Technical Field]

5 **[0001]** The embodiment relates to a display device.

[Background Art]

10 **[0002]** The display market is growing and its application scope is continuously expanding. As the scope of application expands, the resolution and characteristics of products are becoming more diverse.

[0003] As the specifications of products are diversifying, the driving method for display is also becoming more complex accordingly.

[0004] In the case of a driving IC applied to drive a display device, it is designed accordingly. Therefore, the range of applications for design is limited, so that a suitable driver IC is required for each product when necessary.

15 **[0005]** In an existing display device, various methods are applied to secure the characteristics of uniformity. For example, internal compensation is performed by configuring a light-emitting circuit in a pixel (or subpixel), or external compensation is performed in a specific manner.

[0006] Meanwhile, most of the circuit configurations for the operation of the light-emitting circuit have their own capacitors inside the light-emitting circuit, so that constant current characteristics are secured.

20 **[0007]** FIG. 1 is a circuit diagram illustrating an existing light-emitting circuit.

[0008] As shown in FIG. 1, the existing light-emitting circuit includes a driving transistor M1, a scan transistor M2, a sensing transistor M3, and a capacitor CSTG.

25 **[0009]** When the scan transistor M2 is turned on in response to a scan signal SCAN, data signal VDATA is supplied to the driving transistor M1 via the scan transistor M2. The driving transistor M1 supplies the light-emitting current corresponding to the data signal VDATA to the light-emitting element ED, so that the light-emitting element ED emits light.

[0010] The capacitor CSTG supplies the light-emitting current as a constant current to the light-emitting element ED.

[0011] When the sensing transistor M3 is turned on in response to a sensing control signal SEN, the light-emitting current flowing in the driving transistor M1 is detected as a detection signal VSEN. The characteristics of the corresponding light-emitting circuit are calibrated or compensated using the detection signal VSEN.

30 **[0012]** Meanwhile, a light-emitting circuit of an active matrix display device adjusts brightness by applying a pulse amplitude modulation (PWM) method itself or by using the PWM method utilizing a pulse amplitude modulation (PAM) method. In this instance, a capacitor is necessarily provided inside every pixel (or subpixel).

[0013] If the light-emitting circuit is designed so that a capacitor is provided inside every pixel, limitations such as area may occur or additional problems may occur due to the capacitor inside each pixel.

35 [Disclosure]

[Technical Problem]

40 **[0014]** An object of the embodiment is to solve the foregoing and other problems.

[0015] Another object of the embodiment is to provide a display device having a new structure.

[0016] Another object of the embodiment is to provide a display device providing a new driving method.

[0017] Another object of the embodiment is to provide a display device in which a capacitor is not provided in a light-emitting circuit.

45 **[0018]** Another object of the embodiment is to provide a display device that does not require a display driving circuit comprising a converter that converts digital data into analog data.

[0019] The technical problems of the embodiments are not limited to those described in this item and include those that can be understood through the description of the invention.

50 [Technical Solution]

55 **[0020]** According to one aspect of the embodiment to achieve the above or other objects, a display device comprising a plurality of subpixels, comprising: a reference current generation circuit comprising a constant current source configured to generate a reference current; and a plurality of light-emitting circuits provided in the plurality of subpixels and electrically connected to the reference current generation circuit, wherein each of the plurality of light-emitting circuits is configured: to generate a light-emitting current using the reference current to emit light, and to adjust an emission time of the light-emitting element using digital data and a program signal, and wherein the reference current and the light-emitting current are constant currents.

[0021] The reference current generation circuit may comprise: a first transistor connected to the constant current source, and each of the plurality of light-emitting circuits may comprise: a first transistor configured to form a mirror circuit with the first transistor of the reference current generation circuit.

[0022] An aspect ratio of the first transistor of each of the plurality of light-emitting circuits may be greater than or equal to an aspect ratio of the first transistor of the reference current generation circuit.

[0023] The light-emitting element and the first transistor of each of the plurality of light-emitting circuits may be connected between a first power line and a second power line, a first power voltage may be supplied to the first power line, and a second power voltage lower than the first power voltage may be supplied to the second power line.

[0024] The first transistor of the reference current generation circuit and the first transistor of each of the plurality of light-emitting circuits may be NMOS transistors commonly connected to the second power line.

[0025] The first transistor of the reference current generation circuit and the first transistor of each of the plurality of light-emitting circuits may be PMOS transistors commonly connected to the first power line.

[0026] The reference current generation circuit may comprise: a switch connected to the first transistor and configured to turn on/off the reference current.

[0027] Each of the plurality of light-emitting circuits may comprise: a switch connected to the first transistor and configured to turn on/off the light-emitting current.

[0028] A second on-section of the light-emitting current may be included within a first on-section of the reference current.

[0029] Each of the plurality of light-emitting circuits may further comprise: a digital storage configured to generate a control signal for switching the switch of each of the plurality of light-emitting circuits using the digital data.

[0030] The switch of the reference current generation circuit may comprise at least one transistor among a second transistor or a third transistor, and the switch of each of the plurality of light-emitting circuits may comprise at least one transistor among a second transistor or a third transistor.

[0031] The second transistor of the reference current generation circuit and the second transistors of the plurality of light-emitting circuits may be NMOS transistors, and the third transistor of the reference current generation circuit and the third transistor of each of the plurality of light-emitting circuits may be PMOS transistors.

[0032] The constant current source of the reference current generation circuit may comprise a fourth transistor connected to the one or more transistor of the reference current generation circuit.

[0033] The display device may further comprise: a voltage generation circuit connected to the reference current generation circuit and configured to provide a reference voltage for adjusting the reference current.

[0034] The voltage generation circuit may comprise: a plurality of first transistors connected to each other between a third power line and a fourth power line, each of the plurality of first transistors may be diode-connected, and one transistor among the plurality of first transistors may form a current mirror circuit with the fourth transistor of the reference current generation circuit.

[0035] The voltage generation circuit may further comprise: a second transistor connected to another transistor among the plurality of first transistors, and having a gate commonly connected to at least one transistor of the reference current generation circuit.

[0036] The display device of claim 16, further comprise: a current control transistor connected between the one transistor among the plurality of first transistors and the third power line, and having a gate commonly connected to the second transistor of the voltage generation circuit and at least one or more transistor of the reference current generation circuit, and the current control transistor may have a different conductivity type from the at least one or more transistor of the reference current generation circuit.

[0037] The display device may further comprise: a selection switch configured to select one of the reference voltage and an external voltage and output the selected voltage to the reference current generation circuit.

[Advantageous Effects]

[0038] The effects of the display device according to the embodiment are described as follows.

[0039] According to at least one of the embodiments, by copying a reference current generated by a reference current generation circuit to generate a light-emitting current for emitting light of each of the light-emitting elements of a plurality of subpixels, and adjusting an emission time of the light-emitting elements using digital data and a program signal, a capacitors that was required for each subpixel in existing technology is no longer needed, and as the size of the light-emitting circuit gets smaller, the light-emitting area gets larger, thereby increasing the luminance. The circuit structure can be simplified because a converter for converting digital data into an analog voltage is not required.

[0040] According to at least one of the embodiments, an aspect ratio of a transistor of the light-emitting circuit constituting a current mirror circuit may be designed to be greater than an aspect ratio of a transistor of a reference current generation circuit. Accordingly, since the aspect ratio of the transistor of the reference current generation circuit is designed to be small, a relatively small reference current may be generated, thereby reducing the burden on reference current generation, reducing the size of the reference current generation circuit, and reducing power consumption. In

addition, since the light-emitting current of each of the plurality of light-emitting circuits has a large value, the contrast ratio can be improved and high luminance can be implemented.

[0041] According to at least one of the embodiments, a plurality of subpixels may be connected between a first power line and a second power line. Each of the plurality of subpixels may comprise at least one light-emitting element and a light-emitting circuit connected to the light-emitting element. The first power line or the second power line may be commonly connected to the reference current generation circuit and the plurality of light-emitting circuits. In this instance, the transistor of the reference current generation circuit and the transistor of each of the plurality of light-emitting circuits constituting the current mirror circuit may commonly use a second power voltage supplied to the second power line. Accordingly, since the transistor of the reference current generation circuit and the transistor of each of the plurality of light-emitting circuits are simultaneously affected by the IR drop related to the second power voltage, they are not affected by the change in the light-emitting current of each of the plurality of subpixels, so that image quality deterioration can be prevented.

[0042] According to at least one of the embodiments, the reference current generation circuit may generate different reference current based on different reference voltage selected by the selection switches. The reference current generated by the reference current generation circuit may be adjusted in various ways, so that the light-emitting current having the intensity required for each of the plurality of subpixels can be accurately and easily obtained. Accordingly, the luminance can be precisely and accurately controlled, so that the image quality can be improved.

[0043] According to at least one of the embodiments, a gate of one transistor of a voltage generation circuit may be connected to a gate of a second transistor of the reference current generation circuit, so that the gates may be turned on/off simultaneously by the same control signal. For example, during a non-emission-section, i.e., an off-section, one transistor of the voltage generation circuit and the second transistor of the reference current generation circuit may be turned off. Accordingly, since a constant current does not flow in the voltage generation circuit and a reference current does not flow in the reference current generation circuit, power consumption can be reduced.

[0044] According to at least one of the embodiments, a current control transistor may be provided between a transistor of the voltage generation circuit and a transistor of the reference current generation circuit constituting the current mirror circuit, and the current control transistor may have a different conductivity type from a second transistor of the reference current generation circuit. When the current control transistor is turned on during the off-section, the constant current does not flow in the voltage generation circuit and the reference current does not flow in the reference current generation circuit, so that power consumption can be reduced.

[0045] Additional scope of applicability of the embodiments will become apparent from the detailed description that follows. However, since various changes and modifications within the idea and scope of the embodiments may be clearly understood by those skilled in the art, the detailed description and specific embodiments, such as preferred embodiments, should be understood as being given by way of example only.

[Description of Drawings]

[0046]

FIG. 1 is a circuit diagram illustrating an existing light-emitting circuit.

FIG. 2 is a block diagram illustrating a display device according to a first embodiment.

FIG. 3 is a block diagram illustrating a display device according to a second embodiment.

FIG. 4 illustrates a timing diagram according to an embodiment.

FIG. 5 is a block diagram illustrating a display device according to a third embodiment.

FIG. 6 is a block diagram illustrating a display device according to a fourth embodiment.

FIG. 7 is a block diagram illustrating a display device according to a fifth embodiment.

FIG. 8 is a block diagram illustrating a display device according to a sixth embodiment.

FIG. 9 is a block diagram illustrating a display device according to a seventh embodiment.

FIG. 10 is a block diagram illustrating a display device according to an eighth embodiment.

FIG. 11 is a block diagram illustrating a display device according to a ninth embodiment.

FIG. 12 is a block diagram illustrating a display device according to a tenth embodiment.

5 FIG. 13 is a block diagram illustrating a display device according to an eleventh embodiment.

FIG. 14 is a block diagram illustrating a display device according to a twelfth embodiment.

10 FIG. 15 is a block diagram illustrating a display device according to the thirteenth embodiment.

FIG. 16 is a block diagram illustrating a display device according to a fourteenth embodiment.

FIG. 17 illustrates a timing diagram according to an embodiment.

15 **[0047]** The sizes, shapes, dimensions, etc. of elements shown in the drawings can differ from actual ones. In addition, even if the same elements are shown in different sizes, shapes, dimensions, etc. between the drawings, this is only an example on the drawing, and the same elements have the same sizes, shapes, dimensions, etc. between the drawings.

[Mode for Invention]

20 **[0048]** Hereinafter, the embodiment disclosed in this specification will be described in detail with reference to the accompanying drawings, but the same or similar elements are given the same reference numerals regardless of reference numerals, and redundant descriptions thereof will be omitted. The suffixes 'module' and 'unit' for the elements used in the following descriptions are given or used interchangeably in consideration of ease of writing the specification, and do not
25 themselves have a meaning or role that is distinct from each other. In addition, the accompanying drawings are for easy understanding of the embodiment disclosed in this specification, and the technical idea disclosed in this specification is not limited by the accompanying drawings. Also, when an element such as a layer, region or substrate is referred to as being 'on' another element, this means that there can be directly on the other element or be other intermediate elements therebetween.

30 **[0049]** Hereinafter, "~module," "~part," device, etc. may be configured as "~circuit" or "integrated circuit". "~module," "~part," device, etc. may be used interchangeably with "~circuit" or "integrated circuit".

[0050] Hereinafter, although a light-emitting element is described as being provided separately from a light-emitting circuit, the light-emitting element may be included in the light-emitting circuit.

[0051] FIG. 2 is a block diagram illustrating a display device according to a first embodiment.

35 **[0052]** Referring to FIG. 2, the display device according to the first embodiment may comprise a reference current generation circuit 110, a plurality of light-emitting circuits 130-1 to 130-N, a plurality of light-emitting elements 120-1 to 120-N, etc.

[0053] The display device according to the first embodiment may comprise a display panel. The display panel may comprise a plurality of pixels. The display panel may comprise a plurality of subpixels SP-1 to SP-N.

40 **[0054]** Although the drawing illustrates a plurality of subpixels SP-1 to SP-N arranged in a row along a horizontal direction, the plurality of subpixels SP-1 to SP-N may be arranged in a row along a vertical direction or may be arranged in a matrix form.

[0055] The plurality of subpixels SP-1 to SP-N may comprise a plurality of red subpixels, a plurality of green subpixels, and a plurality of blue subpixels. A unit pixel may be configured by adjacent red subpixel, green subpixel, and blue subpixel.
45 In the drawing, SP-1 may be a red subpixel, SP-2 may be a green subpixel, and SP-3 may be a blue subpixel, but are is not limited thereto.

[0056] The red subpixel may emit red light, the green subpixel may emit green light, and the blue subpixel may emit blue light. In addition, the plurality of subpixels SP-1 to SP-N may may further comprise a plurality of transparent subpixels that emit transparent light.

50 **[0057]** Each of the plurality of subpixels SP-1 to SP-N may comprise at least or more light-emitting element 120-1 to 120-N. The light-emitting elements 120-1 to 120-N may comprise an organic light-emitting element, a semiconductor light-emitting element, a micro LED (hereinafter, μ -LED), etc.

[0058] For example, at least or more red light-emitting element for emitting red light may be included in a red subpixel. For example, at least or more green light-emitting element for emitting green light may be included in a green subpixel. For
55 example, at least or more blue light-emitting element for emitting blue light may be included in a blue subpixel.

[0059] A plurality of light-emitting circuits 130-1 to 130-N may be included in a plurality of subpixels SP-1 to SP-N. The plurality of light-emitting circuits 130-1 to 130-N may drive a plurality of light-emitting elements 120-1 to 120-N of the plurality of subpixels SP-1 to SP-N to emit a plurality of color lights. To this end, the plurality of light-emitting circuits 130-1 to

130-N in the plurality of subpixels SP-1 to SP-N may be electrically connected to the plurality of light-emitting elements 120-1 to 120-N.

[0060] The plurality of light-emitting circuits 130-1 to 130-N may generate a plurality of light-emitting currents IEM1 to IEMN for supplying to the plurality of light-emitting elements 120-1 to 120-N. The light-emitting currents IEM1 to IEMN may be referred to as driving currents.

[0061] For example, in the first sub-pixel SP-1, the first light-emitting circuit 130-1 may be electrically connected to the first light-emitting element 120-1, and may supply a first light-emitting current IEM1 to the first light-emitting element 120-1 to drive at least the first light-emitting element 120-1 to emit a first color light. For example, in the second sub-pixel SP-2, the second light-emitting circuit 130-2 may be electrically connected to at least or more second light-emitting element 120-2, and may supply a second light-emitting current IEM2 to the second light-emitting element 120-2 to drive the second light-emitting element 120-2 to emit a second color light. In the third sub-pixel SP-3, the third light-emitting circuit 130-3 may be electrically connected to the third light-emitting element 120-3, and may supply a third light-emitting current IEM3 to the third light-emitting element 120-3 to drive the third light-emitting element 120-3 to emit a third color light. For example, the first color light may be red light, the second color light may be green light, and the third color light may be blue light, but are not limited thereto.

[0062] In the embodiment, the light-emitting circuits 130-1 to 130-N may be implemented as an integrated circuit (hereinafter, referred to as "IC"), a chip, or a package, or may be formed directly on the panel using a semiconductor process. The plurality of light-emitting circuits 130-1 to 130-N may be implemented as individual ICs or may be implemented as one integrated IC.

[0063] In the embodiment, the light-emitting elements 120-1 to 120-N in the subpixels SP-1 to SP-N may be included in the light-emitting circuits 130-1 to 130-N, respectively. That is, the light-emitting elements 120-1 to 120-N may be included in the light-emitting circuits 130-1 to 130-N, and may be implemented as ICs, chips, or packages.

[0064] In the subpixels SP-1 to SP-N, the light-emitting elements 120-1 to 120-N and the light-emitting circuits 130-1 to 130-N may be electrically connected between a first power line 141 and a second power line 142. For example, one side of the respective light-emitting elements 120-1 to 120-N may be electrically connected to the first power line 141, the other side of the respective light-emitting elements 120-1 to 120-N may be connected to one side of the respective light-emitting circuits 130-1 to 130-N, and the other side of the respective light-emitting circuits 130-1 to 130-N may be electrically connected to the second power line 142.

[0065] A first power voltage EVDD may be supplied to the first power line 141, and a second power voltage EVSS may be supplied to the second power line 142. The first power voltage EVDD may be a high-potential voltage, which may be higher than the second power voltage EVSS, which is a low-potential voltage. The second power voltage EVSS may be, for example, grounded or 0 V, but is not limited thereto.

[0066] Meanwhile, the reference current generation circuit 110 may generate a reference current. The reference current generation circuit 110 may be electrically connected to a plurality of subpixels SP-1 to SP-N.

[0067] The reference current may be used to generate a plurality of light-emitting currents IEM1 to IEMN flowing through the plurality of subpixels SP-1 to SP-N. That is, a plurality of light-emitting currents IEM1 to IEMN flowing through the plurality of subpixels SP-1 to SP-N may be generated using the reference current. In an embodiment, the light-emitting currents IEM1 to IEMN corresponding to the reference current may be generated in the plurality of subpixels SP-1 to SP-N, respectively, using a current mirror method. To this end, a current mirror circuit may be configured by a transistor of the reference current generation circuit 110 and a transistor of each of the plurality of light-emitting circuits 130-1 to 130-N. The transistor of the reference current generation circuit 110 may be diode-connected. The transistor of the reference current generation circuit 110 and the transistor of each of the plurality of light-emitting circuits 130-1 to 130-N may have their gates commonly connected.

[0068] The reference current and the light-emitting current IEM1 to IEMN may be constant currents. The constant current may mean that current consistently flows even when the voltage applied to both terminals changes.

[0069] The light-emitting current IEM1 to IEMN may be current corresponding to the reference current. Each of the plurality of light-emitting currents IEM1 to IEMN flowing in the plurality of subpixels SP-1 to SP-N may be equal to or greater than the reference current. That is, the plurality of light-emitting circuits 130-1 to 130-N may generate light-emitting currents IEM1 to IEMN equal to or greater than the reference current according to a preset ratio, that is, a copy ratio.

[0070] The copy ratio may be determined by designing the aspect ratio of each of the transistors of the plurality of light-emitting circuits 130-1 to 130-N differently from the aspect ratio of the transistor of the reference current generation circuit 110.

[0071] For example, when the aspect ratio of each of the transistors of the light-emitting circuits 130-1 to 130-N is the same as the aspect ratio of the transistor of the reference current generation circuit 110, the copy ratio may be 1, so that the light-emitting currents IEM1 to IEMN generated from the plurality of light-emitting circuits 130-1 to 130-N may be the same as the reference current. For example, when the aspect ratio of each of the transistors of the light-emitting circuits 130-1 to 130-N is greater than the aspect ratio of the transistor of the reference current generation circuit 110, the copy ratio may have a value greater than 1, so that the light-emitting currents IEM1 to IEMN generated from the light-emitting circuits

130-1 to 130-N may be greater than the reference current.

[0072] Therefore, since the aspect ratio of each of the transistors of the plurality of light-emitting circuits 130-1 to 130-N is freely designed, the light-emitting currents IEM1 to IEMN required for the subpixels SP-1 to SP-N can be accurately and easily obtained.

[0073] According to the embodiment, the aspect ratio of each of the transistors of the light-emitting circuits 130-1 to 130-N may be designed to be greater than the aspect ratio of the transistor of the reference current generation circuit 110. Therefore, since the aspect ratio of the transistor of the reference current generation circuit 110 is designed to be small, a relatively small reference current may be generated, thereby reducing the burden of generating the reference current, reducing the size of the reference current generation circuit 110, and reducing power consumption. In addition, since the plurality of light-emitting currents IEM1 to IEMN of the plurality of light-emitting circuits 130-1 to 130-N have large values, the contrast ratio can be improved and high luminance can be implemented.

[0074] Meanwhile, the reference current generation circuit 110 may be electrically connected between the third power line 143 and the second power line 142. A third power voltage PVDD may be supplied to the third power line 143. The third power voltage PVDD may be a high-potential voltage and may be different from the first power voltage EVDD. For example, the third power voltage PVDD may be lower than the first power voltage EVDD, but is not limited thereto.

[0075] The second power line 142 may be commonly connected to the reference current generation circuit 110 and the plurality of light-emitting circuits 130-1 to 130-N. In this instance, the transistor of the reference current generation circuit 110 and the plurality of transistors of the plurality of light-emitting circuits 130-1 to 130-N constituting the current mirror circuit may commonly use the second power voltage EVSS supplied to the second power line 142. Therefore, since the transistor of the reference current generation circuit 110 and the plurality of transistors of the plurality of light-emitting circuits 130-1 to 130-N are simultaneously affected by the IR drop related to the second power voltage EVSS, they are not affected by the change in the respective light-emitting currents IEM1 to IEMN of the respective plurality of subpixels SP-1 to SP-N, so that poor image quality can be prevented.

[0076] Meanwhile, the second power line 142 may be commonly connected to the reference current generation circuit 110 and the plurality of light-emitting circuits 130-1 to 130-N, but the third power line 143 may be connected only to the reference current generation circuit 110 and not electrically connected to the plurality of light-emitting circuits 130-1 to 130-N. Accordingly, the reference current may be not affected by the IR drop related to the second power voltage EVSS supplied to the second power line 142, so that an accurate and constant reference current can be obtained.

[0077] Meanwhile, the plurality of light-emitting circuits 130-1 to 130-N may each adjust the on-section (or emission-section) of the light-emitting elements 120-1 to 120-N using digital data and program signals, so that grayscale expression of the image may be possible. For example, the digital data may comprise a signal regarding the on/off of the light-emitting elements 120-1 to 120-N. For example, the digital data may comprise "1" as the on-section of the respective light-emitting elements 120-1 to 120-N, and "0" as the off-section of the respective light-emitting elements 120-1 to 120-N, but are not limited thereto.

[0078] When the light-emitting element 120-1 to 120-N is turned on, the light-emitting element 120-1 to 120-N may emit light, and when the light-emitting element 120-1 to 120-N is turned off, the light-emitting element 120-1 to 120-N may stop emitting light. For example, the program signal may comprise grayscale information, etc. as a control signal for writing input data.

[0079] The light-emitting element 120-1 to 120-N may be turned on according to the digital data, and the on-section of the light-emitting element 120-1 to 120-N may be adjusted according to the program signal, so that an image having a desired grayscale may be displayed. For example, the larger the on-section, the higher the gray level image can be displayed. For the same subpixel SP-1, the corresponding light-emitting element 120-1 to 120-N emit light in different on-sections for each frame, so that an image having different grayscales for each frame may be displayed.

[0080] In the drawing, the node G may be a node between a gate of the transistor of the reference current generation circuit 110 and a gate of each transistor of the plurality of light-emitting circuits 130-1 to 130-N constituting a current mirror circuit.

[0081] A predetermined voltage may be generated at the node G through the transistor of the reference current generation circuit 110 by using the reference current generated in the reference current generation circuit 110. A plurality of light-emitting currents IEM1 to IEMN may be generated in the transistors of the plurality of light-emitting elements 120-1 to 120-N by using the predetermined voltage. In this instance, as described above, since the aspect ratios of the transistors of the light-emitting elements 120-1 to 120-N are each designed to be the same as or different from the aspect ratio of the transistor of the reference current generation circuit 110, the same or different light-emitting currents IEM1 to IEMN may be generated in the transistors of each of the plurality of light-emitting elements 120-1 to 120-N based on the voltage on the node G.

[0082] Meanwhile, in the embodiment, a plurality of subpixels SP-1 to SP-N may be driven simultaneously. That is, the plurality of sub-pixels SP-1 to SP-N may be driven simultaneously within one frame, and the on-sections of the light-emitting elements 120-1 to 120-N of the plurality of sub-pixels SP-1 to SP-N may be adjusted so that images with different grayscales may be displayed on the sub-pixels SP-1 to SP-N, respectively.

[0083] Meanwhile, although not illustrated, the display device according to the first embodiment may comprise a voltage generation circuit. The voltage generation circuit may be connected to the reference current generation circuit 110 and may output a reference voltage for generating a reference current. The reference current generation circuit 110 may generate a reference current based on the reference voltage provided by the voltage generation circuit 150.

[0084] Meanwhile, the display panel may comprise a display area comprising a plurality of pixels (or a plurality of sub-pixels SP-1 to SP-N) and a non-display area excluding the display area.

[0085] The voltage generation circuit 150 and the reference current generation circuit 110 may be provided on the display panel. The voltage generation circuit 150 and the reference current generation circuit 110 may be implemented as one IC or individual ICs.

[0086] The voltage generation circuit 150 and the reference current generation circuit 110 may be provided in an area between adjacent sub-pixels within the display area. For example, the voltage generation circuit 150 and the reference current generation circuit 110 may be provided in the display area.

[0087] The voltage generation circuit 150 and the reference current generation circuit 110 may be provided in one area of the non-display area.

[0088] FIG. 3 is a block diagram illustrating a display device according to a second embodiment. Although the drawing illustrates one subpixel SP-1 among the plurality of subpixels SP-1 to SP-N illustrated in FIG. 2, other subpixels SP-2 to SP-N may also have the same or similar circuit structure as the corresponding subpixel SP-1.

[0089] Referring to FIG. 3, the display device according to the second embodiment may comprise a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, etc. The light-emitting circuit 130-1 and the light-emitting element 120-1 may be included in the subpixel SP-1. Alternatively, the light-emitting circuit 130-1 may not be included in the subpixel SP-1.

[0090] The reference current generation circuit 110 may be electrically connected to the corresponding subpixel SP-1. The reference current generation circuit 110 may be electrically connected to the light-emitting circuit 130-1, so that the light-emitting current IEM1 may be generated in the light-emitting circuit 130-1. That is, the light-emitting current IEM1 may be generated in the corresponding subpixel SP-1 based on the reference current IREF generated by the reference current generation circuit 110, and the light-emitting element 120-1 may be emitted by the generated light-emitting current IEM1.

[0091] The reference current generation circuit 110 may comprise a constant current source 111, a first transistor T1, switches S1 and S2, etc.

[0092] The constant current source 111 may be a source that generates a constant current. In an embodiment, the constant current may be used as the reference current IREF to generate the light-emitting current IEM1 in the light-emitting circuit 130-1.

[0093] The first transistor T1 may be electrically connected to the constant current source 111. The first transistor T1 may be diode-connected. That is, a gate and a drain of the first transistor T1 may be commonly connected. The reference current IREF generated by the constant current source 111 may flow through the first transistor T1.

[0094] The switches S1 and S2 may be connected to the first transistor T1 and may control the on/off of the reference current IREF. The "on" of the reference current IREF may mean that the reference current IREF flows to the first transistor T1, and the "off" of the reference current IREF may mean that the reference current IREF does not flow to the first transistor T1.

[0095] The switch may comprise a first switch S1 and a second switch S2. The first switch S1 may be connected between the first transistor T1 and the second power line 142, and the second switch S2 may be connected between the constant current source 111 and the first transistor T1.

[0096] The first switch S1 and the second switch S2 may be simultaneously turned on or off by first control signals D1 and D2. When the first switch S1 and the second switch S2 are in an open state by the first control signals D1 and D2, the reference current IREF may not flow to the first transistor T1, which may mean that the reference current IREF is turned off. When the first switch S1 and the second switch S2 are in a closed state by the first control signals D1 and D2, the reference current IREF may flow to the first transistor T1, which may mean that the reference current IREF is turned on. A time period during which the reference current IREF flows to the first transistor T1 may be defined as an on-section. A time period during which the reference current IREF does not flow to the first transistor T1 may be defined as an off-section.

[0097] For example, it can be divided into an on-section and an off-section by period. A period can be, for example, one frame, but is not limited thereto. During the on-section, the first switch S1 and the second switch S2 may be in a closed state, so that the reference current IREF may flow to the first transistor T1. During the off-section, the first switch S1 and the second switch S2 may be in an open state, so that the reference current IREF may not flow to the first transistor T1.

[0098] Meanwhile, the light-emitting circuit 130-1 and the light-emitting element 120-1 may be included in the subpixel SP-1. The light-emitting element 120-1 may not be included in the subpixel SP-1.

[0099] The light-emitting circuit 130-1 may drive the light-emitting element 120-1 to emit light. To this end, the light-emitting circuit 130-1 may generate a light-emitting current IEM1, and the light-emitting element 120-1 may emit light in response to the generated light-emitting current IEM1.

[0100] The light-emitting circuit 130-1 may comprise a first transistor T11, switches SW11 and SW12, a digital storage

135-1, etc.

[0101] The first transistor T11 of the light-emitting circuit 130-1 may be connected to the light-emitting element 120-1. The light-emitting element 120-1 and the light-emitting circuit 130-1 may be connected between the first power line 141 and the second power line 142. For example, an anode electrode of the light-emitting element 120-1 may be electrically connected to the first power line 141, a cathode electrode of the light-emitting element 120-1 may be electrically connected to a drain of the first transistor T11, and a source of the first transistor T11 may be electrically connected to the second power line 142.

[0102] The first transistor T11 may generate the light-emitting current IEM1. The light-emitting current IEM1 may be generated based on the reference current IREF generated by the reference current generation circuit 110. The first transistor T11 may generate the light-emitting current IEM1 corresponding to the reference current IREF generated by the reference current generation circuit 110. The first transistor T11 may generate a light-emitting current IEM1 copied from the reference current IREF. When the light-emitting current IEM1 is generated by the first transistor T11, the light-emitting element 120-1 may emit light in response to using the light-emitting current IEM1.

[0103] A current mirror circuit may be configured by the first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1. In the current mirror circuit, the light-emitting current IEM1 may be generated in the first transistor T11 of the light-emitting circuit 130-1 in response to the reference current IREF flowing in the first transistor T1 of the reference current generation circuit 110. At this time, the light-emitting current IEM1 may be equal to or greater than the reference current IREF.

[0104] In an embodiment, the first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 may be MOS transistors. The first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 may be MOS transistors of the same conductivity type. The first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 may be NMOS transistors, but are not limited thereto.

[0105] The first transistor T1 of the reference current generation circuit 110 may be diode-connected, and a gate of the first transistor T1 of the reference current generation circuit 110 and a gate of the first transistor T11 of the light-emitting circuit 130-1 may be commonly connected to the node G. In addition, a source of the first transistor T1 of the reference current generation circuit 110 and a source of the first transistor T11 of the light-emitting circuit 130-1 may be commonly connected to the second power line 142.

[0106] In this instance, the reference current IREF flowing in the reference current generation circuit 110 may be expressed by mathematical formula 1, and the light light-emitting current IEM1 flowing in the light light-emitting circuit 130-1 may be expressed by mathematical formula 2.

[Mathematical formula 1]

$$I_{REF} = \mu \cdot C_{ox} \cdot \frac{W_D}{L_D} \cdot \frac{(V_G - EVSS - V_{TH})^2}{2}$$

[Mathematical formula 2]

$$I_{EM} = \mu \cdot C_{ox} \cdot \frac{W_E}{L_E} \cdot \frac{(V_G - EVSS - V_{TH})^2}{2}$$

[0107] From mathematical formula 1, a voltage V_G of the node G may be calculated. That is, the first transistor T1 of the reference current generation circuit 110 may be a conversion element that converts the reference current IREF into the voltage of the node G.

[0108] The first transistor T11 of the light light-emitting circuit 130-1 may be a conversion element that converts the voltage of the node G into the light light-emitting current IEM1.

[0109] From mathematical formulas 1 and 2, when a process constant (μ , C_{ox}) and an aspect ratio (W_D/L_D and W_E/L_E) of the first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 are the same, the reference current IREF and the light-emitting current IEM1 may be the same. In this instance, the reference current IREF may be copied as it is and generated as the light-emitting current IEM1 in the light-emitting circuit 130-1.

[0110] In contrast, when the process constant (μ , C_{ox}) of the first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 are the same but the aspect ratios (W_D/L_D and W_E/L_E) are different, the reference current IREF and the light-emitting current IEM1 may be different. For example, when the aspect

ratio (W_E/L_E) of the first transistor T11 of the light-emitting circuit 130-1 is greater than the aspect ratio (W_D/L_D) of the first transistor T1 of the reference current generation circuit 110, the light-emitting current IEM1 may be greater than the reference current IREF. For convenience, the aspect ratio (W_D/L_D) of the first transistor T1 of the reference current generation circuit 110 may be named as the first aspect ratio, and the aspect ratio (W_E/L_E) of the first transistor T11 of the light-emitting circuit 130-1 may be named as the second aspect ratio.

[0111] Therefore, the first aspect ratio (W_D/L_D) may be designed to be small, so that a small reference current IREF may be generated in the reference current generation circuit 110. Accordingly, the burden of generating the reference current can be reduced, the size of the reference current generation circuit 110 can be reduced, and power consumption can be reduced.

[0112] In addition, since the second aspect ratio (W_E/L_E) is designed to be large, a large light-emitting current IEM1 may be generated in the light-emitting circuit 130-1. Accordingly, since the light-emitting element 120-1 emits light through the large light-emitting current IEM1, the contrast ratio can be improved and high luminance can be implemented.

[0113] Meanwhile, switches SW11 and SW12 of the light-emitting circuit 130-1 may be connected to the first transistor T11 to control on/off of the light-emitting current IEM1. The switches may comprise a first switch SW11 and a second switch SW12. The first switch SW11 may be connected between the first transistor T11 and the second power line 142, and the second switch SW12 may be connected between the light-emitting element 120-1 and the first transistor T11.

[0114] The first switch SW11 and the second switch SW12 may be turned on or off simultaneously by second control signals C11 and C12. When the first switch SW11 and the second switch SW12 are in an open state by using the second control signals C11 and C12, the light-emitting current IEM1 may not flow to the first transistor T11, which may mean that the light-emitting current IEM1 is turned off. When the first switch SW11 and the second switch SW12 are in a closed state by using the second control signals C11 and C12, the light-emitting current IEM1 may flow to the first transistor T11, which may mean that the light-emitting current IEM1 is turned on. A time period during which the light-emitting current IEM1 flows through the first transistor T11 may be defined as an on-section. A time period during which the light-emitting current IEM1 does not flow through the first transistor T11 may be defined as an off-section.

[0115] For example, it can be divided into an on-section and an off-section by period. The period may be, for example, one frame, but is not limited thereto. During the on-section, the first switch SW11 and the second switch SW12 may be in a closed state, so that the light-emitting current IEM1 may flow through the first transistor T11. During the off-section, the first switch SW11 and the second switch SW12 may be in an open state, so that the light-emitting current IEM1 may not flow through the first transistor T11.

[0116] For convenience of explanation, the on-section in which the reference current IREF flows through the first transistor T1 of the reference current generation circuit 110 may be named as a first on-section SS1, and the on-section in which the light light-emitting current IEM1 flows through the first transistor T11 of the light-emitting circuit 130-1 may be named as a second on-section SS2.

[0117] As illustrated in FIG. 4, when the switches S1 and S2 of the reference current generation circuit 110 are in a closed state in response to the first control signals D1 and D2, the reference current IREF may flow through the first transistor T1 of the reference current generation circuit 110 during the first on-section SS1. When the switches SW11 and SW12 of the light-emitting circuit 130-1 are in a closed state in response to the second control signals C11 and C12, the light light-emitting current IEM1 may flow through the first transistor T11 of the light-emitting circuit 130-1 during the second on-section SS2.

[0118] The second on-section SS2 may be included in the first on-section SS1. The width of the second on-section SS2 may be greater than the width of the first on-section SS1. The rising time of the first on-section SS1 may be faster than the rising time of the second on-section SS2, and the falling time of the first on-section SS1 may be slower than the falling time of the second on-section SS2.

[0119] Meanwhile, the digital storage 135-1 may be included in the light-emitting circuit 130-1, but is not limited thereto.

[0120] The digital storage 135-1 may generate second control signals C11 and C12 for switching the switches SW11 and SW12 of the light-emitting circuit 130-1 using digital data DM-1 and a program signal.

[0121] The switches SW11 and SW12 may be controlled to turn on/off in response to the second control signals C11 and C12. In response to the second control signals C11 and C12, when the switches SW11 and SW12 are in a closed state during the second on-section SS2, the light-emitting current IEM1 may be generated in the first transistor T11, and the light-emitting element 120-1 may emit light in response to the generated light-emitting current IEM1.

[0122] Since the switches SW11 and SW12 are maintained in a closed state during the second on-section SS2, the light-emitting element 120-1 may emit light during the second on-section SS2.

[0123] The second on-section SS2 may be determined by a program signal, but is not limited thereto. The program signal may comprise grayscale information for determining the second on-section SS2. Accordingly, the second control signals C11 and C12 having the second on-section SS2 may be generated based on the digital data DM-1 and the program signal. For example, the larger the grayscale, the larger the second on-section SS2. Accordingly, by changing the width of the second on-section SS2, an image having a desired grayscale may be displayed.

[0124] Meanwhile, first control signals D1 and D2 for maintaining the switches S1 and S2 of the reference current

generation circuit 110 in a closed state during the first on-section SS1 may be provided from an external source, such as a host, a data processing device, a processor, a controller, etc.

[0125] According to an embodiment, a constant current, a light-emitting current IEM1, may be generated from the first transistor T11 of the light-emitting circuit 130-1 in response to the reference current IREF generated by the reference current generation circuit 110. At this time, the second on-section SS2 may be determined or adjusted based on the digital data DM-1 and the program signal, and the light-emitting element 120-1 may emit light during the second on-section SS2, so that an image having different grayscales may be displayed. For example, as the second on-section SS2 increases, an image having a higher grayscale may be displayed.

[0126] FIG. 5 is a block diagram illustrating a display device according to a third embodiment.

[0127] The third embodiment is similar to the second embodiment (FIG. 3) except that the first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 are PMOS transistors. In the third embodiment, the same reference numerals are given to components having the same functions as those of the second embodiment (FIG. 3), and detailed descriptions thereof are omitted. The descriptions omitted in the third embodiment can be easily understood from the description of the second embodiment (FIG. 3).

[0128] Referring to FIG. 5, the display device according to the third embodiment may comprise a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, etc. The light-emitting circuit 130-1 and the light-emitting element 120-1 may be included in the subpixel SP-1. Alternatively, the light-emitting circuit 130-1 may not be included in the subpixel SP-1.

[0129] The reference current generation circuit 110 may comprise a constant current source 111, a first transistor T1, switches S1 and S2, etc.

[0130] The light-emitting circuit 130-1 may comprise a first transistor T11, switches SW11 and SW12, digital storage 135-1, etc.

[0131] Unlike the second embodiment (FIG. 3), in the third embodiment, the first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 may be PMOS transistors.

[0132] In the reference current generation circuit 110, one side of the second switch S2 may be connected to the first power line 141, and the other side of the second switch S2 may be connected to a source of the first transistor T1. A drain of the first transistor T1 may be connected to one side of the first switch S1, the other side of the first switch S1 may be connected to one side of the constant current source 111, and the other side of the constant current source 111 may be connected to the fourth power line 144. A fourth power voltage PVSS may be supplied to the fourth power line 144. The fourth power voltage PVSS may be grounded or 0 V.

[0133] In the light-emitting circuit 130-1, one side of the second switch SW12 may be connected to the first power line 141, and the other side of the second switch SW12 may be connected to a source of the first transistor T11. A drain of the first transistor T11 may be connected to one side of the first switch SW11, the other side of the first switch SW11 may be connected to one side of the light-emitting element 120-1, and the other side of the light-emitting element 120-1 may be connected to the second power line 142.

[0134] Meanwhile, a current mirror circuit may be configured by the first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1.

[0135] To this end, the first transistor T1 of the reference current generation circuit 110 may be diode-connected, and a gate of the first transistor T1 of the reference current generation circuit 110 and a gate of the first transistor T11 of the light-emitting circuit 130-1 may be connected to the node G. In addition, the first power line 141 may be commonly connected to a source of the first transistor T1 of the reference current generation circuit 110 and a source of the first transistor T11 of the light-emitting circuit 130-1.

[0136] In this instance, a voltage of the node G may be obtained by using the reference current IREF flowing in the first transistor T1 of the reference current generation circuit 110, and the light-emitting current IEM1 may be generated in the first transistor T11 of the light-emitting circuit 130-1 based on the voltage of the node G. That is, by the configuration of the current mirror circuit, the reference current IREF of the reference current generation circuit 110 may be copied and generated as the light-emitting current IEM1 in the light-emitting circuit 130-1. At this time, the copy ratio may be defined as a value obtained by dividing the aspect ratio of the first transistor T11 of the light-emitting circuit 130-1, that is, the second aspect ratio (W_E/L_E), by the aspect ratio of the first transistor T1 of the reference current generation circuit 110, that is, the first aspect ratio (W_D/L_D). Since the second aspect ratio (W_E/L_E) is designed to be equal to or greater than the first aspect ratio (W_D/L_D), the light-emitting current IEM1 may be equal to or greater than the reference current IREF.

[0137] A reference current IREF may be generated as a constant current from a constant current source 111 of a reference current generation circuit 110. In this instance, a light-emitting current IEM1 may be generated in a first transistor T11 of a light-emitting circuit 130-1 in response to the reference current IREF flowing in a first transistor T1 of the reference current generation circuit 110. The light-emitting element 120-1 may emit light in response to the generated light-emitting current IEM1. At this time, while the switches SW11 and SW12 are in a closed state in response to the second control signals C11 and C12 provided from the digital storage 135-1, that is, during the second on-section SS2, the light-emitting

element 120-1 may emit light. Therefore, an image of a desired grayscale may be displayed by the light-emitting element 120-1 that emits light during the second on-section SS2.

[0138] FIG. 6 is a block diagram illustrating a display device according to the fourth embodiment.

[0139] The fourth embodiment is the same as the second embodiment (FIG. 3) except for the voltage generation circuit 150. In the fourth embodiment, the same drawing reference numerals are given to components having the same functions as those in the second embodiment (FIG. 3), and detailed descriptions thereof are omitted. The description omitted in the fourth embodiment can be easily understood from the description of the second embodiment (FIG. 3). The fourth embodiment can also be applied to the third embodiment.

[0140] Referring to FIG. 6, the display device according to the fourth embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, etc. The light-emitting circuit 130-1 and the light-emitting element 120-1 may be included in the subpixel SP-1. In contrast, the light-emitting circuit 130-1 may not be included in the subpixel SP-1.

[0141] The reference current generation circuit 110, the light-emitting circuit 130-1, and the light-emitting element 120-1 have already been described, so that detailed descriptions thereof are omitted.

[0142] The voltage generation circuit 150 may be connected to the reference current generation circuit 110 to provide a reference voltage VREF for adjusting or determining the reference current IREF. That is, the reference current IREF generated by the reference current generation circuit 110 may be determined by the reference voltage VREF provided by using the voltage generation circuit 150. For example, the larger the reference voltage VREF, the larger the reference current IREF may be.

[0143] The voltage generation circuit 150 may output the reference voltage VREF to a node X. The reference current generation circuit 110 may generate the reference current IREF based on a voltage of the node X, that is, the reference voltage VREF output from the voltage generation circuit 150.

[0144] For convenience, the node X may be named as the first node, and the node G may be named as the second node, or vice versa.

[0145] According to the fourth embodiment, the voltage generation circuit 150 may provide a reference voltage VREF for adjusting or determining the reference current IREF of the reference current generation circuit 110, so that it can be easy to adjust the reference current IREF of the reference current generation circuit 110.

[0146] Meanwhile, the voltage generation circuit 150 may be equally applied to the third embodiment (FIG. 5).

[0147] FIG. 7 is a block diagram illustrating a display device according to the fifth embodiment.

[0148] The fifth embodiment is the same as the second embodiment (FIG. 3) except for a plurality of subpixels SP-1 to SP-N comprising light-emitting elements 120-1 to 120-N and light-emitting circuits 130-1 to 130-N, respectively. In the fifth embodiment, the same drawing reference numerals are given to components having the same functions as those in the second embodiment (FIG. 3), and detailed descriptions thereof are omitted. The descriptions omitted in the fifth embodiment can be easily understood from the description of the second embodiment (FIG. 3).

[0149] Referring to FIG. 7, the display device according to the fifth embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a plurality of light-emitting circuits 130-1 to 130-N, a plurality of light-emitting elements 120-1 to 120-N, etc.

[0150] A reference current generation circuit 110 and a plurality of sub-pixels SP-1 to SP-N may be provided on a display panel. The plurality of sub-pixels SP-1 to SP-N may be connected between a first power line 141 and a second power line 142.

[0151] The plurality of sub-pixels SP-1 to SP-N may comprise a plurality of light-emitting circuits 130-1 to 130-N, a plurality of light-emitting elements 120-1 to 120-N, etc. One side of each of the plurality of light-emitting elements 120-1 to 120-N may be electrically connected to a first power line 141, the other side of each of the plurality of light-emitting elements 120-1 to 120-N may be electrically connected to one side of each of the plurality of light-emitting circuits 130-1 to 130-N, and the other side of each of the plurality of light-emitting circuits 130-1 to 130-N may be electrically connected to a second power line 142.

[0152] The plurality of light-emitting circuits 130-1 to 130-N may each comprise first transistors T11 to TN1, switches SW11 to SWN1 and SW12 to SWN2, digital storages 135-1 to 135-N, etc.

[0153] The switch may comprise first switches SW11 to SWN1 and/or second switches SW12 to SWN2. For example, the first switches SW11 to SWN1 may be connected between sources of the first transistors T11 to TN1 and the second power line 142, and the second switches SW12 to SWN2 may be connected between drains of the first transistors T11 to TN1 and the plurality of light-emitting elements 120-1 to 120-N.

[0154] Meanwhile, the reference current generation circuit 110 may be electrically connected to the plurality of subpixels SP-1 to SP-N.

[0155] The reference current generation circuit 110 may comprise a constant current source 111, a first transistor T1, switches S1 and S2, etc.

[0156] The switch may comprise a first switch S1 and/or a second switch S2. For example, the first switch S1 may be connected between a source of the first transistor T1 and the second power line 142, and the second switch S2 may be

connected between a drain of the first transistor T1 and the constant current source 111.

[0157] A current mirror circuit may be configured by the first transistor T1 of the reference current generation circuit 110 and the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N. The first transistor T1 of the reference current generation circuit 110 and the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N may be NMOS transistors.

[0158] The first transistor T1 of the reference current generation circuit 110 may be diode-connected. A gate of the first transistor T1 of the reference current generation circuit 110 and gates of the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N may be commonly connected to the node G. The second power line 142 may be commonly connected to the reference current generation circuit 110 and the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N.

[0159] In this instance, the reference current IREF generated in the reference current generation circuit 110 may be copied, so that the plurality of light-emitting currents IEM1 to IEMN may be generated in the plurality of light-emitting circuits 130-1 to 130-N of the plurality of subpixels SP-1 to SP-N. At this time, the plurality of light-emitting currents IEM1 to IEMN may be the same or different depending on the copy ratio. When the copy ratio is 1, the plurality of light-emitting currents IEM1 to IEMN may all be the same and may also be the same as the reference current IREF. When the copy ratio is different, the plurality of light-emitting currents IEM1 to IEMN may be different. When the copy ratio is greater than 1, the plurality of light-emitting currents IEM1 to IEMN may be greater than the reference current IREF.

[0160] Therefore, the aspect ratios (W_E/L_E) of the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N may be designed to be the same or different with respect to the aspect ratio (W_D/L_D) of the first transistor T1 of the reference current generation circuit 110, so that the plurality of light-emitting circuits 130-1 to 130-N may generate the same or different plurality of light-emitting currents IEM1 to IEMN. The plurality of light-emitting currents IEM1 to IEMN may be constant currents.

[0161] According to the fifth embodiment, a plurality of light-emitting currents IEM1 to IEMN for emitting light of a plurality of light-emitting elements 120-1 to 120-N of a plurality of subpixels SP-1 to SP-N may be generated simultaneously by using a reference current IREF generated from a single reference current generation circuit 110, thereby greatly simplifying the circuit structure and making it easy and highly efficient to drive a plurality of subpixels SP-1 to SP-N.

[0162] According to the fifth embodiment, a plurality of copy ratios of a plurality of light-emitting circuits 130-1 to 130-N may be adjusted to generate a plurality of identical or different light-emitting currents IEM1 to IEMN in each of a plurality of light-emitting circuits 130-1 to 130-N of a plurality of subpixels SP-1 to SP-N, thereby improving image quality through optimal grayscale expression or optimal luminance implementation.

[0163] FIG. 8 is a block diagram illustrating a display device according to the sixth embodiment.

[0164] The sixth embodiment is the same as the fourth embodiment (FIG. 6) except that the switch S1 of the reference current generation circuit 110 and the switch SW11 of the light-emitting circuit 130-1 are provided one of each. In the sixth embodiment, the same drawing symbols are given to components having the same functions as in the fourth embodiment (FIG. 6), and detailed descriptions thereof are omitted. The descriptions omitted in the sixth embodiment can be easily understood from the description of the fourth embodiment (FIG. 6). The sixth embodiment can also be applied to the fifth embodiment.

[0165] Referring to FIG. 8, the display device according to the sixth embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, etc.

[0166] The second switch S2 of the reference current generation circuit 110 and the second switch SW12 of each of the light-emitting circuits 130-1 provided in the fourth embodiment (FIG. 6) can be omitted in the sixth embodiment.

[0167] A current mirror circuit may be configured by a first transistor T1 of the reference current generation circuit 110 and a first transistor T11 of the light-emitting circuit 130-1. The first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 may be NMOS transistors.

[0168] In the reference current generation circuit 110, the constant current source 111 may comprise a PMOS transistor. In this instance, the third power line 143 may be commonly connected to the voltage generation circuit 150 and the reference current generation circuit 110.

[0169] In the reference current generation circuit 110, a drain of the first transistor T1 may be directly connected to the constant current source 111. In the reference current generation circuit 110, a source of the first transistor T1 may be electrically connected to one side of the first switch S1, and the other side of the first switch S1 may be connected to the second power line 142.

[0170] In the light-emitting circuit 130-1, a drain of the first transistor T11 may be directly connected to the light-emitting element 120-1. In the light-emitting circuit 130-1, a source of the first transistor T11 may be connected to one side of the first switch SW11, and the other side of the first switch SW11 may be connected to the second power line 142.

[0171] As illustrated in FIG. 4, the first switch S1 of the reference current generation circuit 110 may be in a closed state during the first on-section SS1, and the first switch SW11 of the light-emitting circuit 130-1 may be in a closed state during the second on-section SS2. Accordingly, the light-emitting element 120-1 may emit light at least during the second on-

section SS2, so that an image having a grayscale corresponding to the second on-section SS2 may be displayed.

[0172] FIG. 9 is a block diagram illustrating a display device according to the seventh embodiment.

[0173] The seventh embodiment is the same as the fourth embodiment (FIG. 6) except that the switch S2 of the reference current generation circuit 110 and the switch SW12 of the light-emitting circuit 130-1 are provided one of each. In the seventh embodiment, the same drawing reference numerals are assigned to components having the same functions as in the fourth embodiment (FIG. 6), and detailed descriptions thereof are omitted. The description omitted in the seventh embodiment can be easily understood from the description of the fourth embodiment (FIG. 6). The seventh embodiment can also be applied to the fifth embodiment.

[0174] Referring to FIG. 9, the display device according to the seventh embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, etc.

[0175] The first switch S1 of the reference current generation circuit 110 and the first switch SW11 of each of the light-emitting circuits 130-1 provided in the fourth embodiment (FIG. 6) can be omitted in the seventh embodiment.

[0176] A current mirror circuit may be configured by a first transistor T1 of the reference current generation circuit 110 and a first transistor T11 of the light-emitting circuit 130-1. The first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 may be NMOS transistors.

[0177] In the reference current generation circuit 110, one side of the second switch S2 may be electrically connected to the constant current source 111, the other side of the second switch S2 may be electrically connected to a drain of the first transistor T1, and a source of the first transistor T1 may be directly connected to the second power line 142.

[0178] In the light-emitting circuit 130-1, one side of the second switch SW12 may be electrically connected to the light-emitting element 120-1, the other side of the second switch SW12 may be electrically connected to a drain of the first transistor T11, and a source of the first transistor T11 may be directly connected to the second power line 142.

[0179] As illustrated in FIG. 4, the second switch S2 of the reference current generation circuit 110 may be in a closed state during the first on-section SS1, and the second switch SW12 of the light-emitting circuit 130-1 may be in a closed state during the second on-section SS2. Accordingly, the light-emitting element 120-1 may emit light during at least the second on-section SS2, and an image having a grayscale corresponding to the second on-section SS2 may be displayed.

[0180] FIG. 10 is a block diagram illustrating a display device according to the eighth embodiment.

[0181] The eighth embodiment is similar to the fourth embodiment (FIG. 6) except that the first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 are PMOS transistors. In the eighth embodiment, the same drawing reference numerals are given to components having the same functions as those in the fourth embodiment (FIG. 6), and detailed descriptions thereof are omitted. Descriptions omitted in the eighth embodiment can be easily understood from the description of the fourth embodiment (FIG. 6). The eighth embodiment can be equally applied to the fifth embodiment (FIG. 7), the sixth embodiment (FIG. 8), and the seventh embodiment (FIG. 9).

[0182] Referring to FIG. 10, the display device according to the eighth embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, etc.

[0183] The reference current generation circuit 110 and the light-emitting circuit 130-1 may each be provided with two switches S1 and S2 and SW11 and SW12, but may also be provided with one switch.

[0184] A current mirror circuit may be configured by a first transistor T1 of the reference current generation circuit 110 and a first transistor T11 of the light-emitting circuit 130-1. The first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 may be PMOS transistors. In this instance, the first power line 141 may be commonly connected to one side of the reference current generation circuit 110 and one side of the light-emitting circuit 130-1. The other side of the reference current generation circuit 110 may be electrically connected to the fourth power line 144, and the other side of the light-emitting circuit 130-1 may be electrically connected to the second power line 142.

[0185] In the reference current generation circuit 110, the constant current source 111 may comprise an NMOS transistor. In this instance, the fourth power line 144 may be commonly connected to the voltage generation circuit 150 and the reference current generation circuit 110.

[0186] In the reference current generation circuit 110, one side of the second switch S2 may be electrically connected to the first power line 141, and the other side of the second switch S2 may be electrically connected to a source of the first transistor T1. A drain of the first transistor T1 may be electrically connected to one side of the first switch S1, the other side of the first switch S1 may be electrically connected to one side of the constant current source 111, and the other side of the constant current source 111 may be electrically connected to the fourth power line 144.

[0187] FIG. 11 is a block diagram illustrating a display device according to the ninth embodiment.

[0188] The ninth embodiment is similar to the fourth embodiment (FIG. 6) except for a selection switch 161. In the ninth embodiment, the same drawing reference numerals are given to components having the same functions as those in the fourth embodiment (FIG. 6), and detailed descriptions thereof are omitted. The descriptions omitted in the ninth embodiment can be easily understood from the description of the fourth embodiment (FIG. 6). The ninth embodiment

can be equally applied to the fifth embodiment (FIG. 7), the sixth embodiment (FIG. 8), and the seventh embodiment (FIG. 9).

[0189] Referring to FIG. 11, the display device according to the ninth embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, a selection switch 161, etc.

[0190] Since the voltage generation circuit 150, the reference current generation circuit 110, the light-emitting circuit 130-1, and the light-emitting element 120-1 have already been described, a detailed description thereof will be omitted.

[0191] In the reference current generation circuit 110, the constant current source 111 may comprise a PMOS transistor. In this instance, the third power line 143 may be commonly connected to the voltage generation circuit 150 and the reference current generation circuit 110.

[0192] The selection switch 161 may select one of the reference voltage VREF and the external voltage VON and output the selected voltage to the reference current generation circuit 110.

[0193] The selection switch 161 may be configured as an analog multiplexer. The analog multiplexer may be configured to comprise at least or more NMOS transistor and at least or more PMOS transistor.

[0194] As illustrated in FIG. 11, the reference voltage VREF may be provided from the voltage generation circuit 150. The external voltage VON may be provided from a host, a data processing device, a processor, a controller, etc.

[0195] Although the drawing illustrates that one external voltage VON is provided, a plurality of external voltages that are different from each other may be provided, and one of the plurality of external voltages as well as the reference voltage VREF may be selected by the selection switch 161.

[0196] The selection switch 161 may be connected between the voltage generation circuit 150 and the reference current generation circuit 110. For example, a first input side of the selection switch 161 may be electrically connected to an output side of the voltage generation circuit 150, and a second input side of the selection switch 161 may be electrically connected to a output side of an external device such as a host. An output side of the selection switch 161 may be electrically connected to the constant current source 111 of the reference current generation circuit 110 through the node X.

[0197] According to the ninth embodiment, the reference current generation circuit 110 may generate different reference currents IREF based on different reference voltages VREF selected by the selection switch 161. Since the reference current IREF generated by the reference current generation circuit 110 may be variously adjusted, the light-emitting current IEM1 having the intensity required in the subpixel SP-1 may be accurately and easily obtained. Accordingly, the luminance can be precisely and accurately controlled, so that the image quality may be improved.

[0198] FIG. 12 is a block diagram illustrating a display device according to the tenth embodiment.

[0199] The tenth embodiment is similar to the ninth embodiment (Fig. 11) except that the first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 are PMOS transistors. In addition, the tenth embodiment is the same as the eighth embodiment (Fig. 10) except for the selection switch 162. In the tenth embodiment, the same drawing reference numerals are given to components having the same functions as those of the eighth embodiment (Fig. 10) and the ninth embodiment (Fig. 11), and detailed descriptions thereof are omitted. Descriptions omitted in the tenth embodiment can be easily understood from the descriptions of the eighth embodiment (Fig. 10) and the ninth embodiment (Fig. 11).

[0200] Referring to FIG. 12, the display device according to the tenth embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, a selection switch 162, etc.

[0201] Since the voltage generation circuit 150, the reference current generation circuit 110, the light-emitting circuit 130-1, and the light-emitting element 120-1 have already been described, a detailed description thereof will be omitted.

[0202] In the reference current generation circuit 110, the constant current source 111 may comprise an NMOS transistor. In this instance, the fourth power line 144 may be commonly connected to the voltage generation circuit 150 and the reference current generation circuit 110.

[0203] The selection switch 162 may select one of the reference voltage VREF and the external voltage VON and output the selected voltage to the reference current generation circuit 110.

[0204] As illustrated in FIG. 12, the reference voltage VREF may be provided from the voltage generation circuit 150. The external voltage VON may be provided from a host, a data processing device, a processor, a controller, etc.

[0205] Although the drawing illustrates that one external voltage VON is provided, plurality of external voltages that are different from each other may be provided, and one of the plurality of external voltages as well as the reference voltage VREF may be selected by the selection switch 162.

[0206] The selection switch 162 may be connected between the voltage generation circuit 150 and the reference current generation circuit 110. For example, a first input side of the selection switch 162 may be electrically connected to an output side of the voltage generation circuit 150, and a second input side of the selection switch 162 may be electrically connected to an output side of an external device such as a host. An output side of the selection switch 162 may be electrically connected to a constant current source 111 of the reference current generation circuit 110 via an node X.

[0207] According to the tenth embodiment, the reference current generation circuit 110 may generate different reference

currents IREF based on different reference voltages VREF selected by the selection switch 162. Since the reference current IREF generated by the reference current generation circuit 110 may be variously adjusted, the light-emitting current IEM1 having the intensity required for the subpixel SP-1 can be accurately and easily obtained. Accordingly, the luminance can be precisely and accurately controlled, so that the image quality can be improved.

[0208] FIG. 13 is a block diagram illustrating a display device according to the eleventh embodiment.

[0209] The eleventh embodiment embodies the voltage generation circuit 150, the reference current generation circuit 110, and the light-emitting circuit 130-1, respectively, and is similar to the fourth embodiment (FIG. 6). In the eleventh embodiment, the same drawing reference numerals are given to components having the same functions as in the fourth embodiment (FIG. 6), and detailed descriptions thereof are omitted. The description omitted in the eleventh embodiment can be easily understood from the description of the fourth embodiment (FIG. 6).

[0210] Referring to FIG. 13, the display device according to the eleventh embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, etc.

[0211] The voltage generation circuit 150 may comprise a plurality of first transistors 151 to 153 connected in series between the third power line 143 and the fourth power line 144. Although three first transistors 151 to 153 are illustrated in the drawing, four or more may be provided.

[0212] The first transistors 151 to 153 may be PMOS transistors, but may also be NMOS transistors.

[0213] The plurality of first transistors 151 to 153 may each be diode-connected. The diode-connected first transistors 151 to 153 may be applied with a predetermined voltage corresponding to a threshold voltage. Accordingly, a constant current may flow to the voltage generation circuit 150 corresponding to a voltage in which a predetermined voltage is added as many as the number of first transistors 151 to 153.

[0214] Meanwhile, one transistor 151 of the plurality of first transistors 151 to 153 may form a current mirror circuit with a fourth transistor T4 of the reference current generation circuit 110. That is, a gate of one transistor 151 of the plurality of first transistors 151 to 153 and a gate of the fourth transistor T4 of the reference current generation circuit 110 may be commonly connected to the node X. One transistor 151 of the plurality of first transistors 151 to 153 may output a reference voltage VREF to the node X using a constant current. The fourth transistor T4 of the reference current generation circuit 110 may generate a reference current IREF based on the reference voltage VREF.

[0215] The constant current flowing in the voltage generation circuit 150 and the reference current IREF flowing in the reference current generation circuit 110 may be expressed by mathematical formulas similar to mathematical formulas 1 and 2, respectively. Accordingly, the reference current IREF may be the same as or different from the constant current flowing in the voltage generation circuit 150.

[0216] As the number of the plurality of first transistors 151 to 153 of the voltage generation circuit 150 increases, the reference voltage VREF may increase, and the reference current IREF generated in the reference current generation circuit 110 may also increase. Therefore, when the target reference current IREF to be obtained from the reference current generation circuit 110 is determined, the number of the plurality of first transistors 151 to 153 of the voltage generation circuit 150 and the threshold voltage, etc. may be determined so that the target reference current IREF may be generated.

[0217] Meanwhile, the reference current generation circuit 110 may comprise a first transistor T1, a second transistor T2, a third transistor T3, and a fourth transistor T4, which are connected in series between the third power line 143 and the second power line 142. For example, the first transistor T1 and the second transistor T2 may be NMOS transistors, and the third transistor T3 and the fourth transistor T4 may be PMOS transistors, but are not limited thereto.

[0218] The first transistor T1 may be connected between the second transistor T2 and the third transistor T3, and may form a current mirror circuit with the first transistor T11 of the light-emitting circuit 130-1. The first transistor T1 may be an NMOS transistor, but may also be a PMOS transistor.

[0219] The second transistor T2 may be included in the first switch S1 illustrated in FIGS. 3, 5 to 8, 10, and 11. The second transistor T2 may be connected between the first transistor T1 and the second power line 142. As illustrated in FIG. 4, the second transistor T2 may be turned on during the first on-section SS1 of the reference current IREF, so that the reference current IREF may flow to the first transistor T1.

[0220] The third transistor T3 may be included in the second switch S2 illustrated in FIG. 3, FIGS. 5 to 7, and FIGS. 9 to 11. The third transistor T3 may be connected between the first transistor T1 and the fourth transistor T4. The third transistor T3 may be turned on during the first on-section SS1 of the reference current IREF, so that the reference current IREF may flow to the first transistor T1.

[0221] The second transistor T2 and the third transistor T3 may be different conductivity transistors. That is, the second transistor T2 may be an NMOS transistor, and the third transistor may be a PMOS transistor, but are not limited thereto.

[0222] The second transistor T2 and the third transistor T3 may be turned on and turned off simultaneously by first control signals D1 and D2, but is not limited thereto. For example, the second transistor T2 may be turned on by the first control signal D1 of a high level, and the third transistor T3 may be turned on by the first control signal D2 of a low level. For example, the second transistor T2 and the third transistor T3 may be turned on simultaneously during the on-section, and turned off simultaneously during the off-section.

[0223] The fourth transistor T4 may be included in the constant current source 111 illustrated in FIGS. 3 and 5 to 12.

[0224] The fourth transistor T4 may be connected between the third power line 143 and the third transistor T3. The fourth transistor T4 may form a current mirror circuit with one transistor 151 of the plurality of first transistors T1 of the voltage generation circuit 150. In this instance, the constant current generated in the voltage generation circuit 150 may be copied to generate a reference current IREF in the reference current generation circuit 110. In other words, the reference voltage VREF converted by the constant current of the voltage generation circuit 150 may be output to the node G, and the reference current IREF may be generated in the reference current generation circuit 110 based on the reference voltage VREF.

[0225] Meanwhile, the light-emitting element 120-1 and the light-emitting circuit 130-1 may be connected between the first power line 141 and the second power line 142.

[0226] The light-emitting circuit 130-1 may comprise a first transistor T11, a second transistor T12, and a third transistor T13 connected in series with each other between the light-emitting element 120-1 and the second power line 142.

[0227] The first transistor T11 may be connected between the second transistor T12 and the third transistor T13, and may form a current mirror circuit with the first transistor T1 of the reference current generation circuit 110. The first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 may be NMOS transistors, but may also be PMOS transistors.

[0228] The second transistor T12 may be included in the first switch SW11 illustrated in FIGS. 3, 5 to 8, 10, and 11. The second transistor T12 may be connected between the first transistor T11 and the second power line 142. As illustrated in FIG. 4, the second transistor T12 may be turned on during the second on-section SS2 of the light-emitting current IEM1, so that the light-emitting current IEM1 may be supplied to the light-emitting element 120-1 to emit light.

[0229] The third transistor T13 may be included in the second switch SW12 illustrated in FIG. 3, FIG. 5 to 7, and FIG. 9 to FIG. 11. The third transistor T13 may be connected between the first transistor T11 and the light-emitting element 120-1. The third transistor T13 may be turned on during the first on-section SS1 of the light-emitting current, so that the light-emitting current may be supplied to the light-emitting element 120-1 to emit light.

[0230] The second transistor T12 and the third transistor T13 may be different conductive transistors. For example, the second transistor T12 may be an NMOS transistor, and the third transistor T13 may be a PMOS transistor, but are not limited thereto.

[0231] The second transistor T12 and the third transistor T13 may be turned on and turned off simultaneously by second control signals C11 and C12, but are not limited thereto. For example, the second transistor T12 may be turned on by the second control signal C11 of a high level, and the third transistor T13 may be turned on by the second control signal C12 of a low level. For example, the second transistor T12 and the third transistor T13 may be turned on simultaneously during the on-section and turned off simultaneously during the off-section.

[0232] For convenience of explanation, the current mirror circuit configured by the first transistor 151 of the voltage generation circuit 150 and the fourth transistor T4 of the reference current generation circuit 110 may be named a first current mirror circuit. The current mirror circuit formed by the first transistor T1 of the reference current generation circuit 110 and the first transistor T11 of the light-emitting circuit 130-1 may be referred to as the second current mirror circuit.

[0233] FIG. 14 is a block diagram illustrating a display device according to the twelfth embodiment.

[0234] The twelfth embodiment is the same as the eleventh embodiment (FIG. 13) except for a second transistor 154 of the voltage generation circuit 150 and a current control transistor 170. In the twelfth embodiment, the same drawing reference numerals are given to components having the same functions as in the eleventh embodiment (FIG. 13), and detailed descriptions thereof are omitted. The descriptions omitted in the twelfth embodiment can be easily understood from the description of the eleventh embodiment (FIG. 13).

[0235] Referring to FIG. 14, the display device according to the twelfth embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, a current control transistor 170, etc.

[0236] Since the reference current generation circuit 110, the light-emitting circuit 130-1, and at least or more light-emitting element 120-1 have already been described, a detailed description thereof will be omitted.

[0237] The voltage generation circuit 150 may comprise a plurality of first transistors 151 to 153 and a second transistor 154 between a third power line 143 and a fourth power line 144.

[0238] The plurality of first transistors 151 to 153 may be diode-connected, respectively.

[0239] One of the plurality of first transistors 151 to 153 may form a current mirror circuit with a fourth transistor T4 of the reference current generation circuit 110.

[0240] The second transistor 154 may be connected between the last transistor 153 of the plurality of first transistors 151 to 153 and the fourth power line 144, but is not limited thereto.

[0241] A gate of the second transistor 154 of the voltage generation circuit 150 may be electrically connected to a gate of the second transistor T2 of the reference current generation circuit 110. The second transistor 154 of the voltage generation circuit 150 and the second transistor T2 of the reference current generation circuit 110 may be the same conductivity type transistors. For example, the second transistor 154 of the voltage generation circuit 150 and the second

transistor T2 of the reference current generation circuit 110 may be NMOS transistors. Therefore,

[0242] Therefore, the second transistor 154 of the voltage generation circuit 150 and the second transistor T2 of the reference current generation circuit 110 may be turned on/off simultaneously by the first control signal D1. For example, the second transistor 154 and the second transistor T2 may be turned on simultaneously by the first control signal D1 of a high level. For example, the second transistor 154 and the second transistor T2 may be turned off simultaneously by the first control signal D1 of a low level.

[0243] For example, the second transistor 154 of the voltage generation circuit 150 and the second transistor T2 of the reference current generation circuit 110 may be turned on during one period, for example, the first on-section SS1 of the frame, and turned off during the other period, i.e., the off-section. When the second transistor 154 of the voltage generation circuit 150 and the second transistor T2 of the reference current generation circuit 110 are turned off, the constant current may not flow in the voltage generation circuit 150 and the reference current IREF may not flow in the reference current generation circuit 110. Accordingly, power consumption may be reduced by preventing the constant current or the reference current IREF from flowing during the off section for each period.

[0244] Meanwhile, the current control transistor 170 may be connected between one transistor 151 of the plurality of first transistors 151 to 153 and the third power line 143. A gate of the current control transistor 170 may be commonly connected to a gate of the second transistor 154 of the voltage generation circuit 150 and a gate of the second transistor T2 of the reference current generation circuit 110.

[0245] The current control transistor 170 may have a different conductivity type from the second transistor T2 of the reference current generation circuit 110. For example, the second transistor T2 of the reference current generation circuit 110 may be an NMOS transistor, and the current control transistor 170 may be a PMOS transistor.

[0246] In this instance, when the second transistor T2 of the reference current generation circuit 110 is turned on, the current control transistor 170 may be turned off. For example, the second transistor 154 of the voltage generation circuit 150 and the second transistor T2 of the reference current generation circuit 110 may be turned on by the first control signal D1 of a high level, but the current control transistor 170 may be turned off.

[0247] When the second transistor T2 of the reference current generation circuit 110 is turned off, the current control transistor 170 may be turned on. For example, the second transistor 154 of the voltage generation circuit 150 and the second transistor T2 of the reference current generation circuit 110 may be turned off by the first control signal D1 of the low level, but the current control transistor 170 may be turned on.

[0248] For example, when the second transistor T2 of the reference current generation circuit 110 is turned off during the off-section of one period, the current control transistor 170 may be turned on so that the third power voltage PVDD supplied to the third power line 143 may be output to the node X. In this instance, since the gate and source of the transistor 151 of the voltage generation circuit 150 and the gate and source of the fourth transistor T4 of the reference current generation circuit 110 constituting the current mirror circuit have the same voltage, a constant current does not flow in the voltage generation circuit 150 and a reference current IREF does not flow in the reference current generation circuit 110. Therefore, power consumption can be reduced by preventing the constant current or reference current IREF from flowing during the off-section for each period.

[0249] FIG. 15 is a block diagram illustrating a display device according to the thirteenth embodiment.

[0250] The thirteenth embodiment is the same as the twelfth embodiment (FIG. 14) except for a plurality of subpixels SP-1 to SP-N comprising light-emitting elements 120-1 to 120-N and light-emitting circuits 130-1 to 130-N, respectively. In the thirteenth embodiment, the same drawing reference numerals are given to components having the same functions as in the twelfth embodiment (FIG. 14), and detailed descriptions thereof are omitted. The descriptions omitted in the thirteenth embodiment can be easily understood from the description of the twelfth embodiment (FIG. 14).

[0251] Referring to FIG. 15, the display device according to the thirteenth embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a plurality of light-emitting circuits 130-1 to 130-N, a plurality of light-emitting elements 120-1 to 120-N, a current control transistor 170, etc.

[0252] Since the voltage generation circuit 150, the reference current generation circuit 110, and the current control transistor 170 have already been described, a detailed description thereof will be omitted.

[0253] The reference current generation circuit 110 and a plurality of sub-pixels SP-1 to SP-N may be provided on a display panel. The plurality of sub-pixels SP-1 to SP-N may be connected between a first power line 141 and a second power line 142.

[0254] In this instance, the plurality of subpixels SP-1 to SP-N may comprise a plurality of light-emitting circuits 130-1 to 130-N, a plurality of light-emitting elements 120-1 to 120-N, etc. One side of each of the plurality of light-emitting elements 120-1 to 120-N may be electrically connected to a first power line 141, the other side of each of the plurality of light-emitting elements 120-1 to 120-N may be electrically connected to one side of each of the light-emitting circuits 130-1 to 130-N, and the other side of each of the light-emitting circuits 130-1 to 130-N may be electrically connected to a second power line 142.

[0255] The plurality of light-emitting circuits 130-1 to 130-N may comprise a plurality of first transistors T11 to TN1, a plurality of second transistors T12 to TN2, a plurality of third transistors T13 to TN3, a plurality of digital storages 135-1 to 135-N, etc. In the light-emitting circuits 130-1 to 130-N, one of the second transistors T12 to TN2 and the third transistors

T13 to TN3 may be omitted.

[0256] Meanwhile, the reference current generation circuit 110 may be electrically connected to a plurality of subpixels SP-1 to SP-N. The reference current generation circuit 110 may be electrically connected to a plurality of light-emitting circuits 130-1 to 130-N of the plurality of subpixels SP-1 to SP-N. The reference current generation circuit 110 may copy the reference current IREF to generate light-emitting currents IEM1 to IEMN in the plurality of light-emitting circuits 130-1 to 130-N, respectively.

[0257] The reference current generation circuit 110 may comprise the first transistor T1 to the fourth transistor T4. The first transistor T1 of the reference current generation circuit 110 may form a current mirror circuit with the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N. For example, the first transistor T1 of the reference current generation circuit 110 and the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N may be NMOS transistors, but may also be PMOS transistors.

[0258] The plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N may each generate the plurality of light-emitting currents IEM1 to IEMN in response to the reference current IREF flowing through the first transistor T1 of the reference current generation circuit 110. When the plurality of copy ratios of the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N are the same, the plurality of light-emitting currents IEM1 to IEMN flowing through the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N may be the same. When the plurality of copy ratios of the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N are 1, the plurality of light-emitting currents IEM1 to IEMN flowing through the plurality of first transistors T11 to TN1 of the plurality of light-emitting circuits 130-1 to 130-N may be equal to the reference current IREF flowing through the first transistor T1 of the reference current generation circuit 110.

[0259] According to the thirteenth embodiment, the plurality of light-emitting currents IEM1 to IEMN for emitting the plurality of light-emitting elements 120-1 to 120-N of the plurality of sub-pixels SP-1 to SP-N may be simultaneously generated using the reference current IREF generated by one reference current generation circuit 110, thereby greatly simplifying the circuit structure and making it easy and highly efficient to drive the plurality of sub-pixels SP-1 to SP-N.

[0260] According to the thirteenth embodiment, since the copy ratio is adjusted, desired light-emitting currents IEM1 to IEMN may be generated in the plurality of light-emitting circuits 130-1 to 130-N of the plurality of subpixels SP-1 to SP-N, respectively, so that the image quality can be improved through optimal grayscale expression or optimal luminance implementation.

[0261] FIG. 16 is a block diagram illustrating a display device according to a fourteenth embodiment.

[0262] The fourteenth embodiment embodies the digital storage 135-1 and is similar to the thirteenth embodiment (FIG. 15). In the fourteenth embodiment, the same drawing reference numerals are assigned to components having the same functions as in the thirteenth embodiment (FIG. 15), and detailed descriptions thereof are omitted. The descriptions omitted in the fourteenth embodiment can be easily understood from the description of the thirteenth embodiment (FIG. 15).

[0263] Referring to FIG. 16, the display device according to the fourteenth embodiment may comprise a voltage generation circuit 150, a reference current generation circuit 110, a light-emitting circuit 130-1, at least or more light-emitting element 120-1, a current control transistor 170, etc.

[0264] Since the voltage generation circuit 150, the reference current generation circuit 110, the light-emitting circuit 130-1, and the current control transistor 170 have already been described, a detailed description thereof will be omitted.

[0265] The light-emitting circuit 130-1 may comprise a first transistor T11, a second transistor T12, and a third transistor T13 connected in series with each other, and a digital storage 135-1. The first transistor T11 of the light-emitting circuit 130-1 may form a current mirror circuit with the first transistor T1 of the reference current generation circuit 110. One of the second transistor T12 and the third transistor T13 in the light-emitting circuit 130-1 may be omitted.

[0266] The digital storage 135-1 may comprise a latch circuit. As illustrated in FIG. 16, the latch circuit may comprise an inverter element, a pair of NMOS transistors, a pair of PMOS transistors, a pair of switches, etc.

[0267] Digital data DM-1 and a program signal PS1 may be input to the digital storage 135-1, i.e., the latch circuit. The program signal PS1 may be a control signal for writing input data to the latch circuit. A pair of switches may be turned on/off by the program signal PS1.

[0268] The digital storage 135-1 may generate second control signals C11 and C12 having a second on-section SS2 based on the on/off information of the digital data DM-1 and the grayscale information of the program signal PS1, and output the generated second control signals C11 and C12 to the second transistor T12 and the third transistor T13. Therefore, as illustrated in FIG. 17, in response to the second control signals C11 and C12, the second transistor T12 and the third transistor T13 may be turned on, so that the light-emitting element 120-1 may emit light in response to the light-emitting current IEM1 supplied during the second on-section SS2.

[0269] Meanwhile, in response to the first control signals D1 and D2, the second transistor T2 and the third transistor T3 of the reference current generation circuit 110 may be turned on, so that the reference current IREF may flow to the reference current generation circuit 110 during the first on-section SS1. The second on-section SS2 may be included in the first on-section SS1.

[0270] The first on-section SS1 and the second on-section SS2 may be called the first emission-section and the second emission-section, respectively.

[0271] The above detailed description should not be construed as limiting in all respects and should be considered illustrative. The scope of the embodiment should be determined by reasonable interpretation of the appended claims, and all changes within the equivalent range of the embodiment are included in the scope of the embodiment.

Claims

1. A display device comprising a plurality of subpixels, comprising:

a reference current generation circuit comprising a constant current source configured to generate a reference current; and
a plurality of light-emitting circuits provided in the plurality of subpixels and electrically connected to the reference current generation circuit,
wherein each of the plurality of light-emitting circuits is configured:

to generate a light-emitting current using the reference current to emit light, and
to adjust an emission time of the light-emitting element using digital data and a program signal, and
wherein the reference current and the light-emitting current are constant currents.

2. The display device of claim 1, wherein the reference current generation circuit comprises:

a first transistor connected to the constant current source, and
wherein each of the plurality of light-emitting circuits comprises:
a first transistor configured to form a mirror circuit with the first transistor of the reference current generation circuit.

3. The display device of claim 2, wherein an aspect ratio of the first transistor of each of the plurality of light-emitting circuits is greater than or equal to an aspect ratio of the first transistor of the reference current generation circuit.

4. The display device of claim 2, wherein the light-emitting element and the first transistor of each of the plurality of light-emitting circuits are connected between a first power line and a second power line,

wherein a first power voltage is supplied to the first power line, and
wherein a second power voltage lower than the first power voltage is supplied to the second power line.

5. The display device of claim 4, wherein the first transistor of the reference current generation circuit and the first transistor of each of the plurality of light-emitting circuits are NMOS transistors commonly connected to the second power line.

6. The display device of claim 4, wherein the first transistor of the reference current generation circuit and the first transistor of each of the plurality of light-emitting circuits are PMOS transistors commonly connected to the first power line.

7. The display device of claim 2, wherein the reference current generation circuit comprises:
a switch connected to the first transistor and configured to turn on/off the reference current.

8. The display device of claim 7, wherein each of the plurality of light-emitting circuits comprises:
a switch connected to the first transistor and configured to turn on/off the light-emitting current.

9. The display device of claim 8, wherein a second on-section of the light-emitting current is included within a first on-section of the reference current.

10. The display device of claim 8, wherein each of the plurality of light-emitting circuits further comprises:
a digital storage configured to generate a control signal for switching the switch of each of the plurality of light-emitting circuits using the digital data.

11. The display device of claim 8, wherein the switch of the reference current generation circuit comprises at least or more

transistor among a second transistor or a third transistor, and
wherein the switch of each of the plurality of light-emitting circuits comprises at least or more transistor among a second transistor or a third transistor.

5 **12.** The display device of claim 11, wherein the second transistor of the reference current generation circuit and the second transistors of the plurality of light-emitting circuits are NMOS transistors, and
wherein the third transistor of the reference current generation circuit and the third transistor of each of the plurality of light-emitting circuits are PMOS transistors.

10 **13.** The display device of claim 11, wherein the constant current source of the reference current generation circuit comprises a fourth transistor connected to the one or more transistor of the reference current generation circuit.

14. The display device of claim 13, further comprises:
a voltage generation circuit connected to the reference current generation circuit and configured to provide a
15 reference voltage for adjusting the reference current.

15. The display device of claim 14, wherein the voltage generation circuit comprises:

20 a plurality of first transistors connected to each other between a third power line and a fourth power line,
wherein each of the plurality of first transistors is diode-connected, and
wherein one transistor among the plurality of first transistors is configured to form a current mirror circuit with the fourth transistor of the reference current generation circuit.

16. The display device of claim 14, wherein the voltage generation circuit further comprises:
25 a second transistor connected to another transistor among the plurality of first transistors, and having a gate commonly connected to at least or more transistor of the reference current generation circuit.

17. The display device of claim 16, further comprises:

30 a current control transistor connected between the one transistor among the plurality of first transistors and the third power line, and having a gate commonly connected to the second transistor of the voltage generation circuit and at least one or more transistor of the reference current generation circuit, and
wherein the current control transistor has a different conductivity type from the at least or more transistor of the
35 reference current generation circuit.

18. The display device of claim 14, further comprises:
a selection switch configured to select one of the reference voltage and an external voltage and output the selected
40 voltage to the reference current generation circuit.

FIG. 1

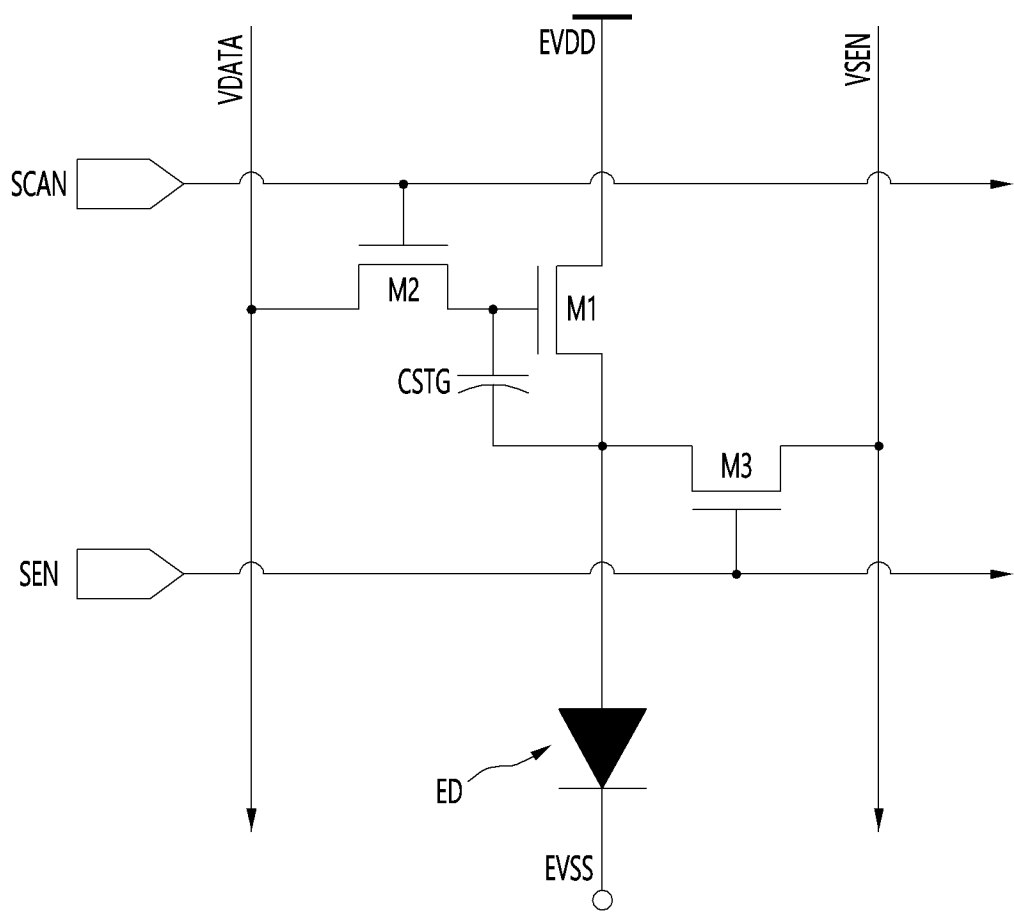


FIG. 2

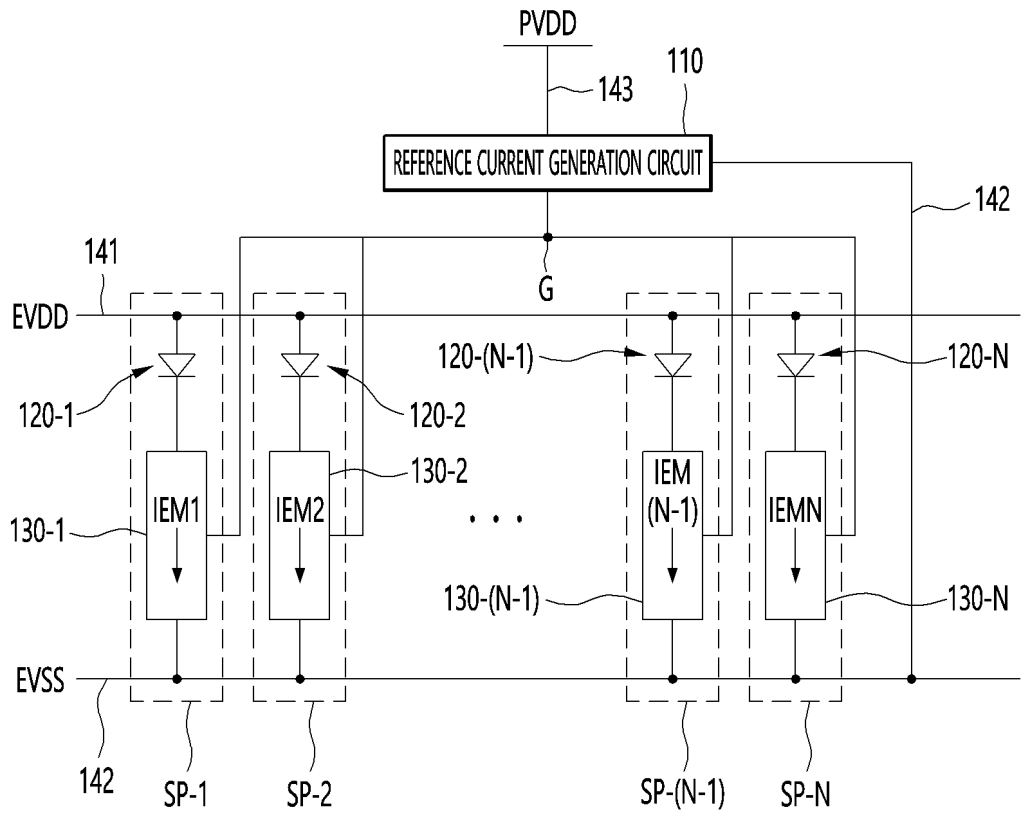


FIG. 3

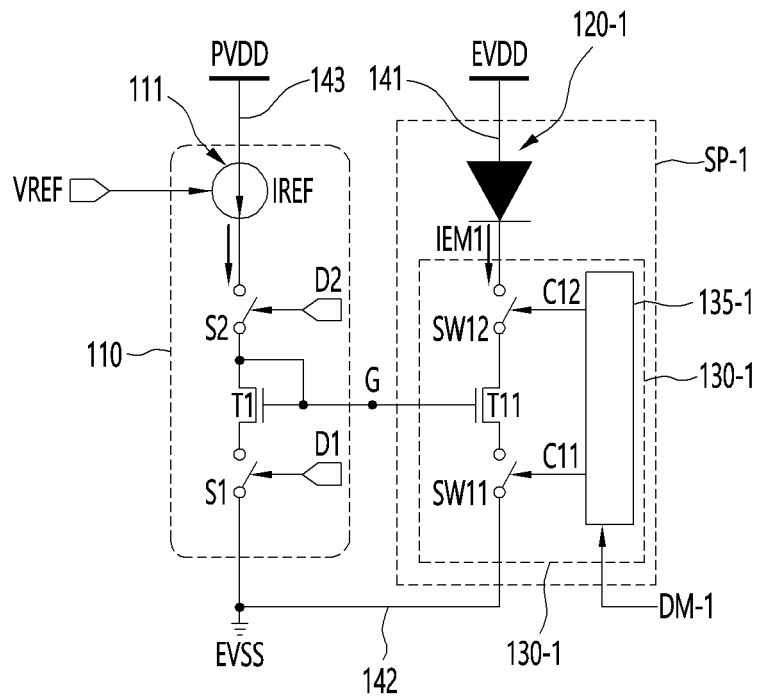


FIG. 4

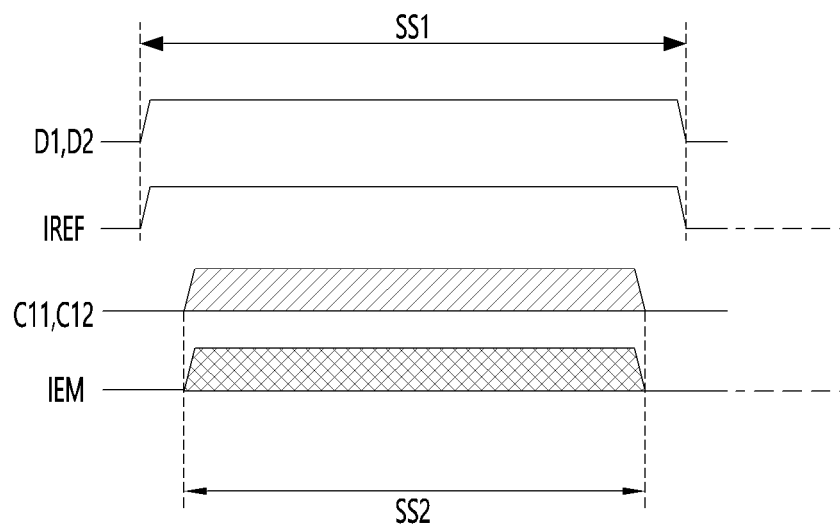


FIG. 5

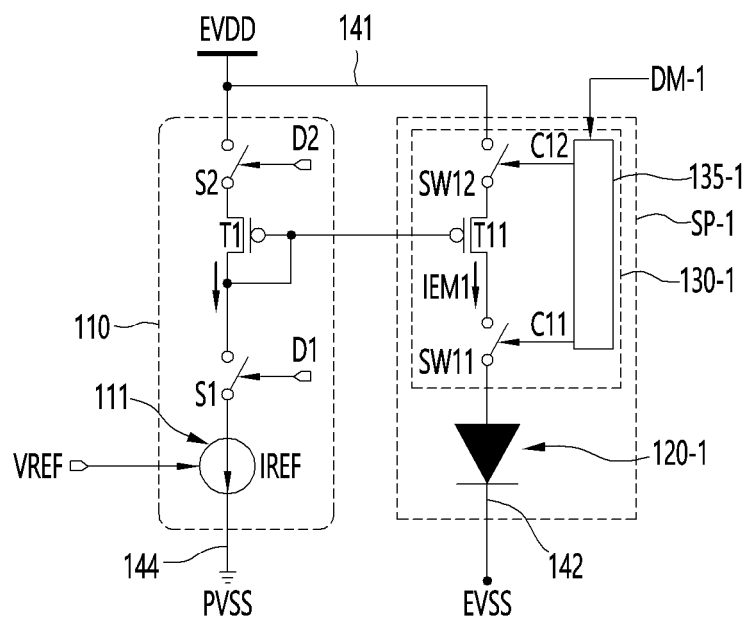


FIG. 6

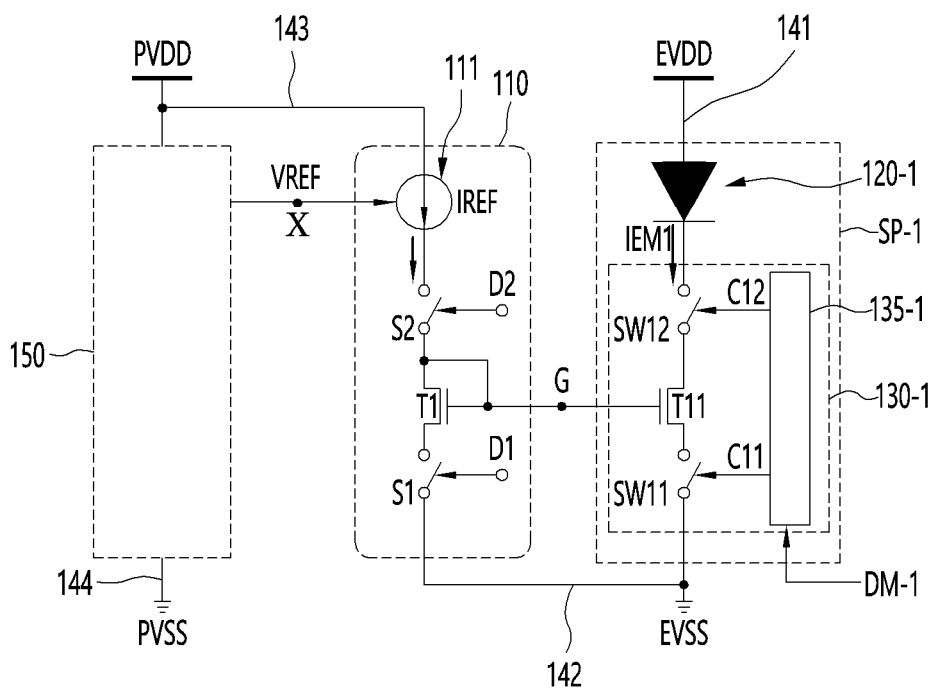


FIG. 7

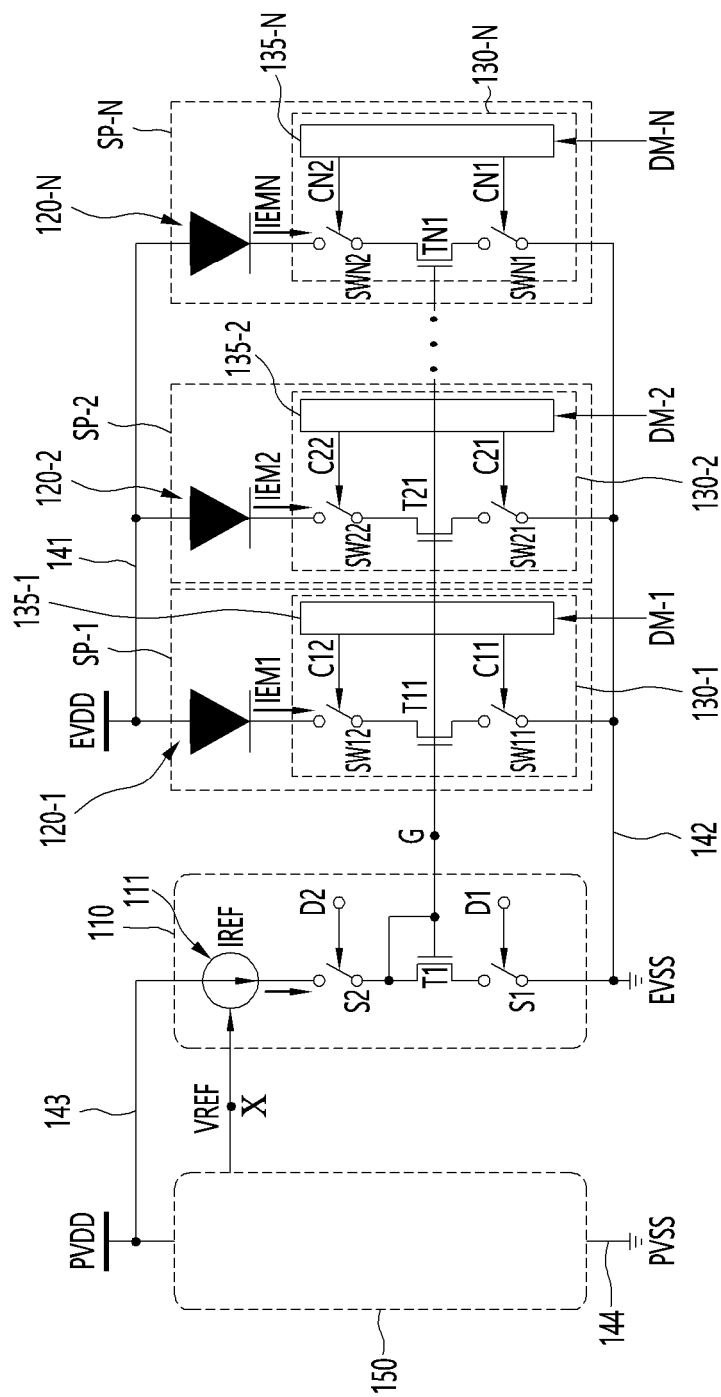


FIG. 8

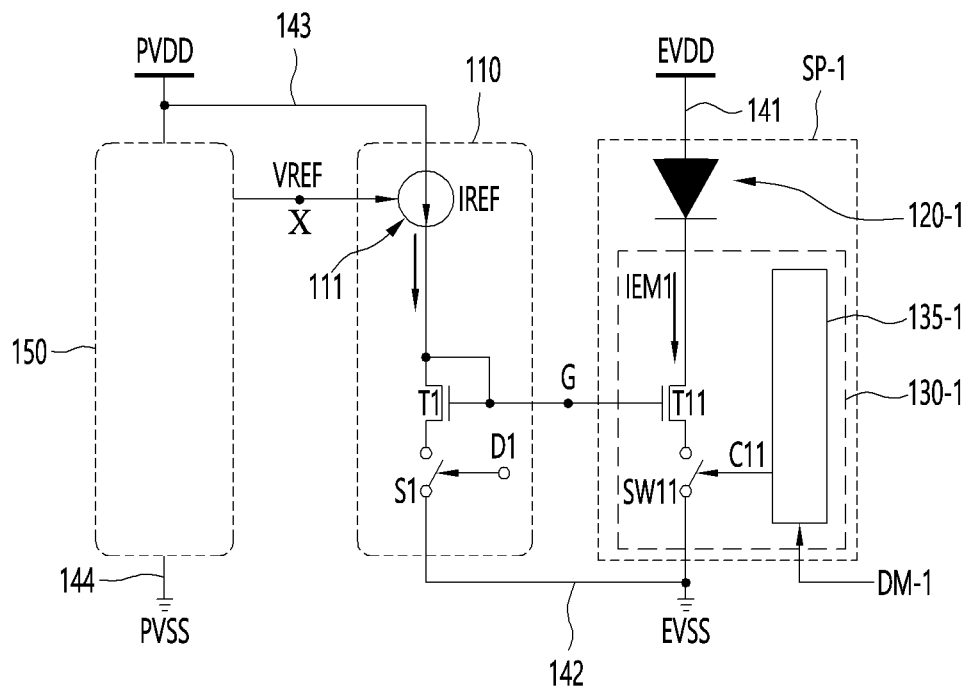


FIG. 9

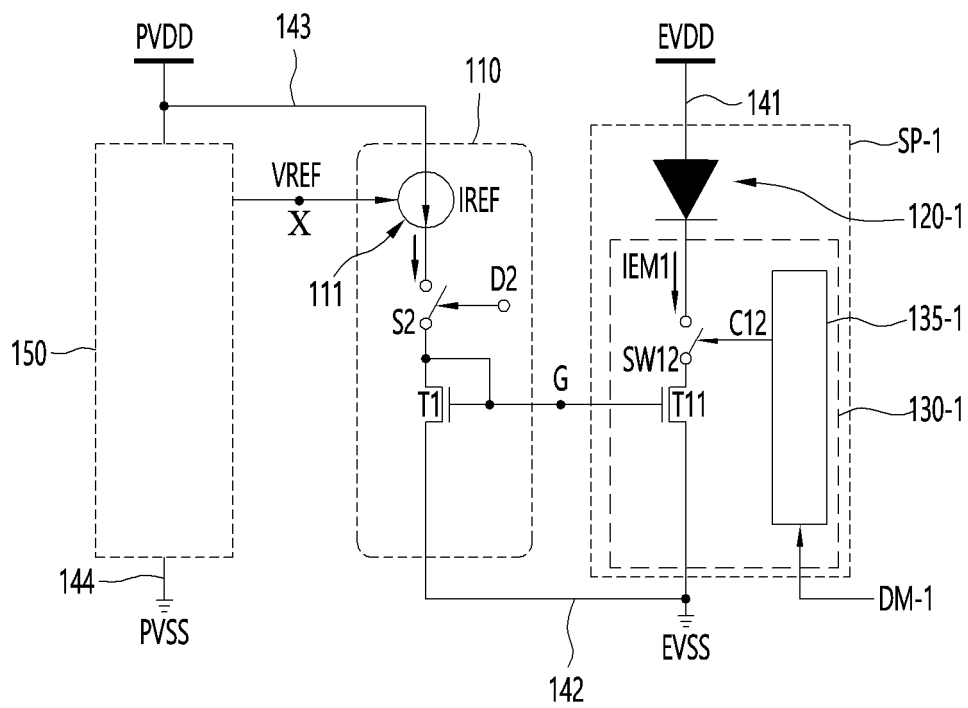


FIG. 10

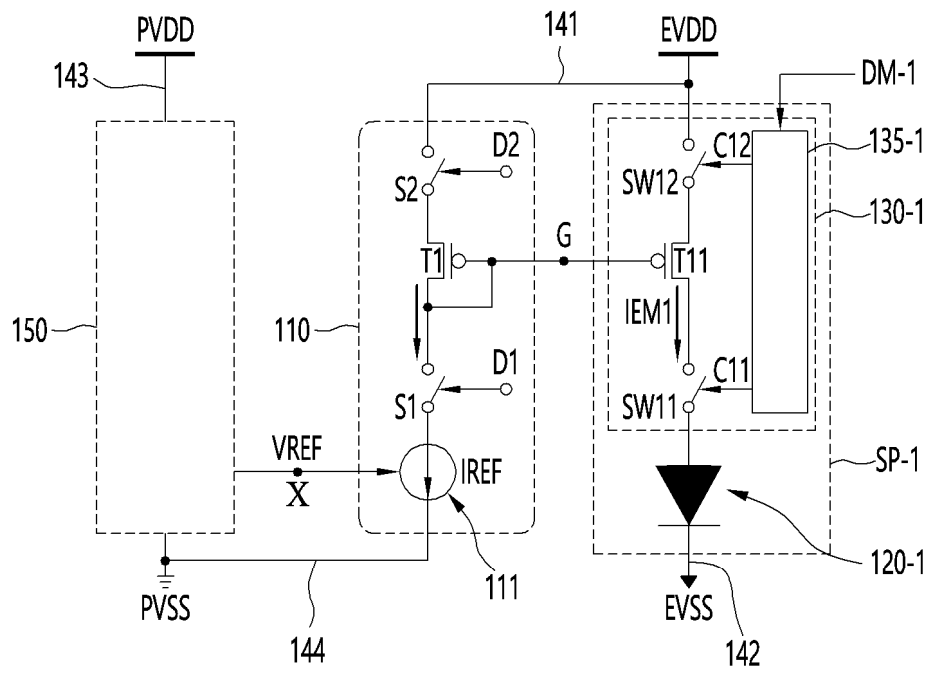


FIG. 11

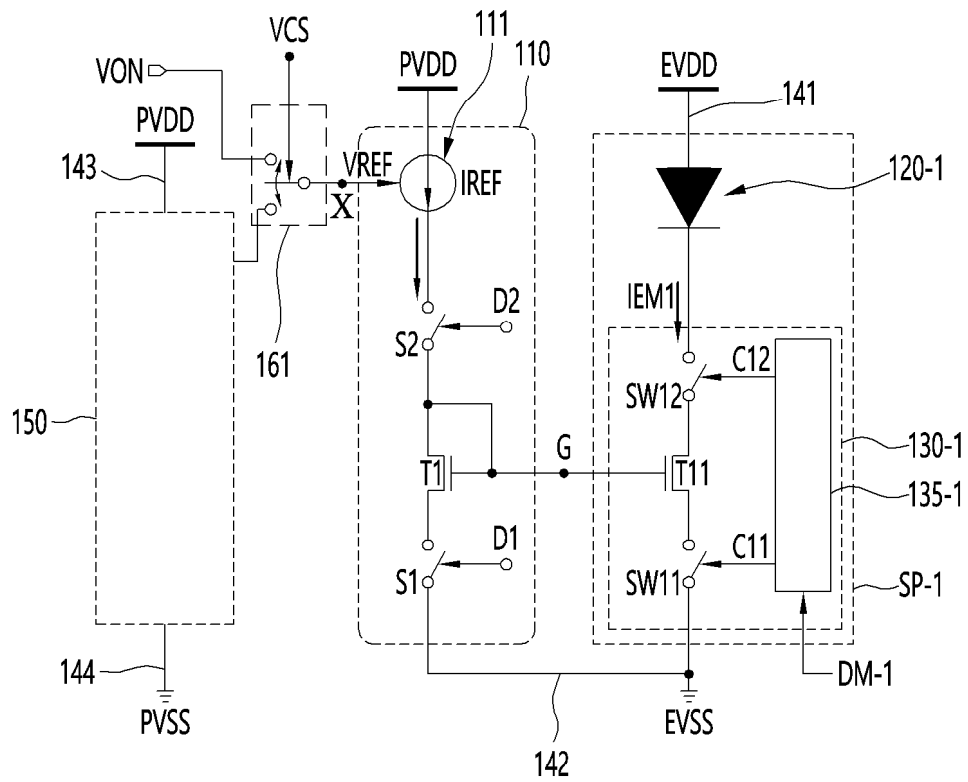


FIG. 12

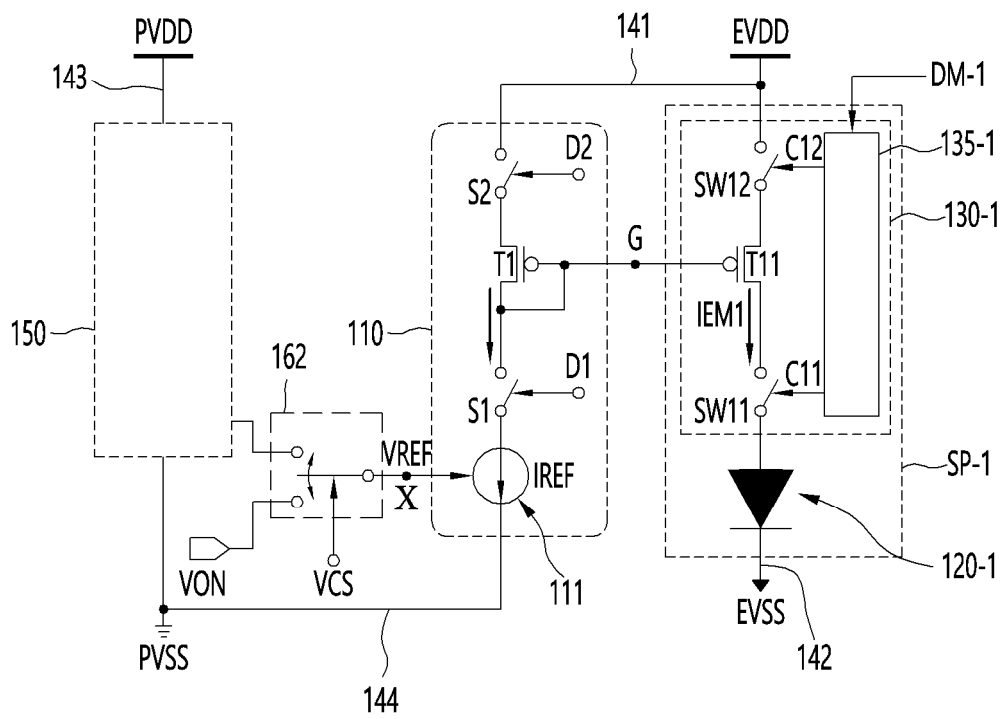


FIG. 13

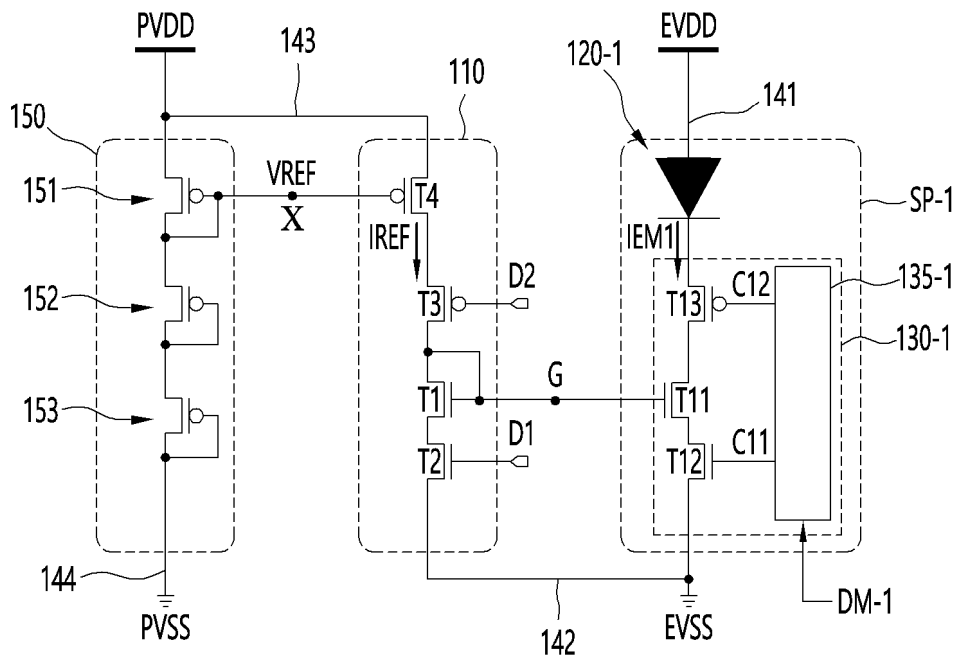


FIG. 14

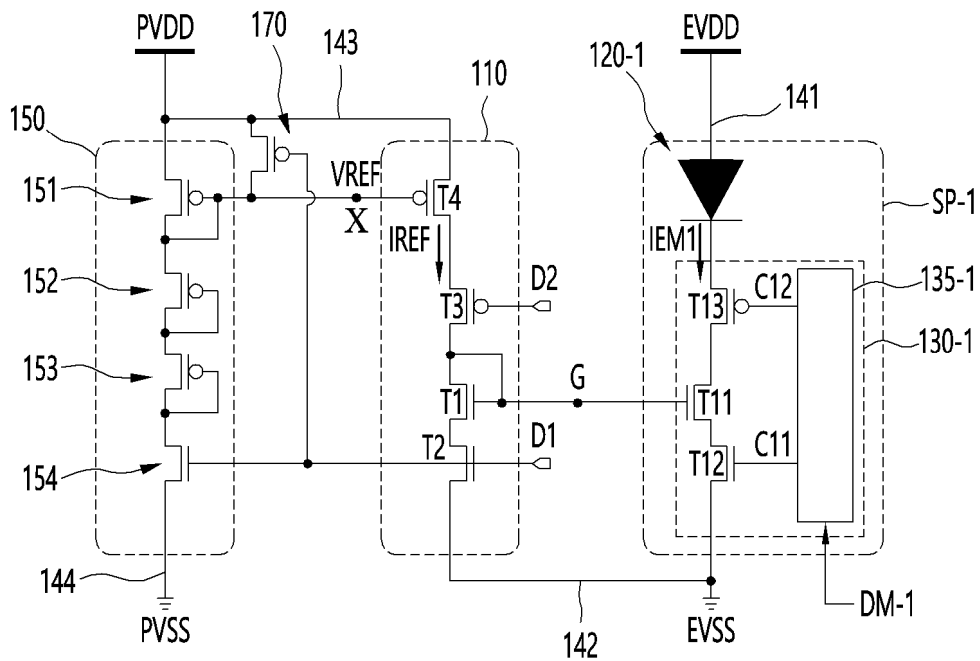


FIG. 15

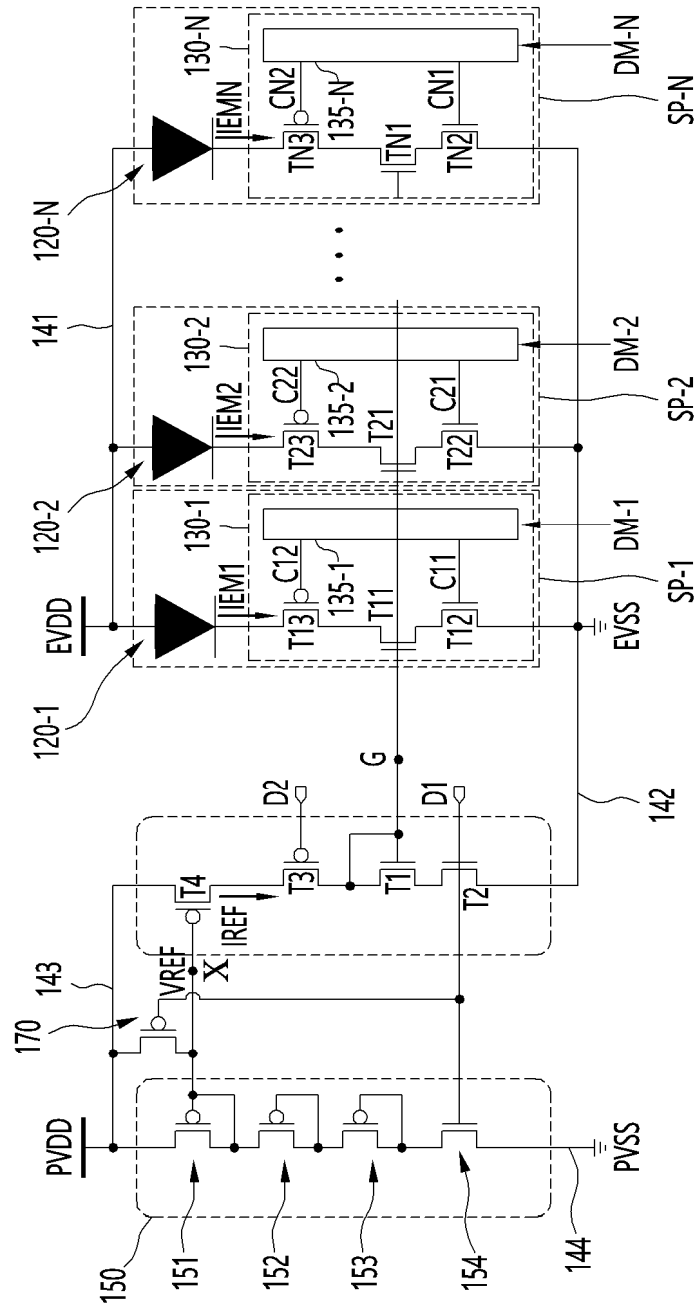


FIG. 16

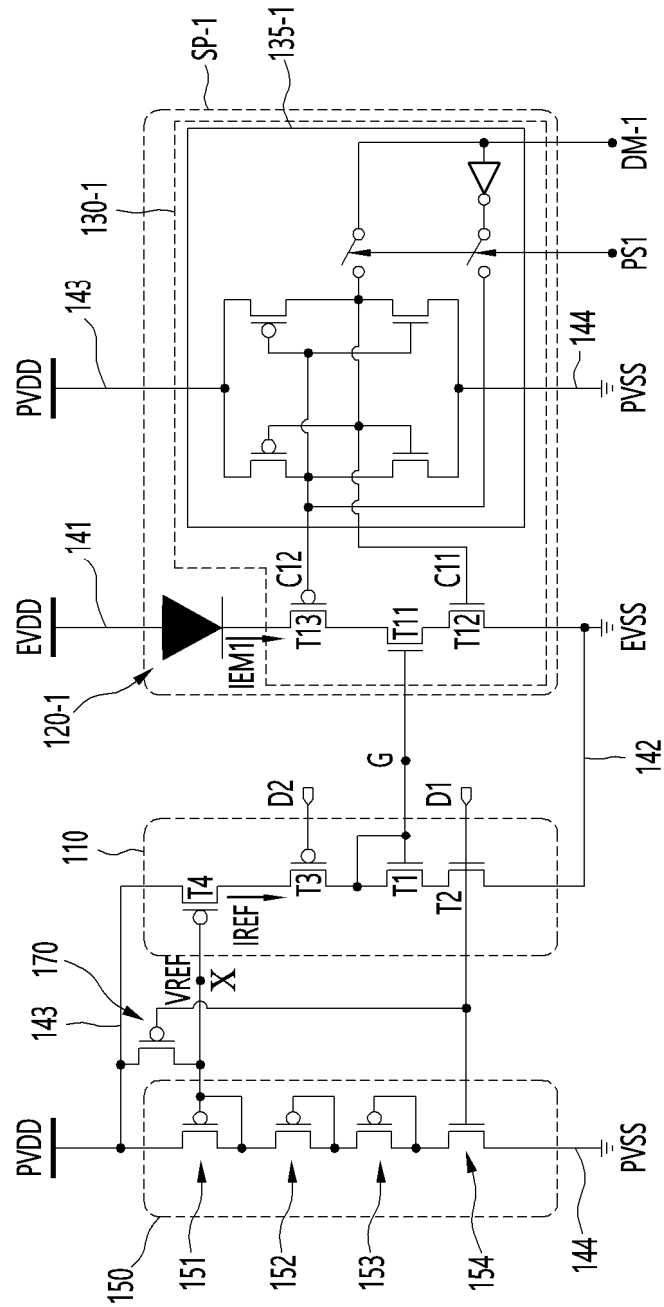
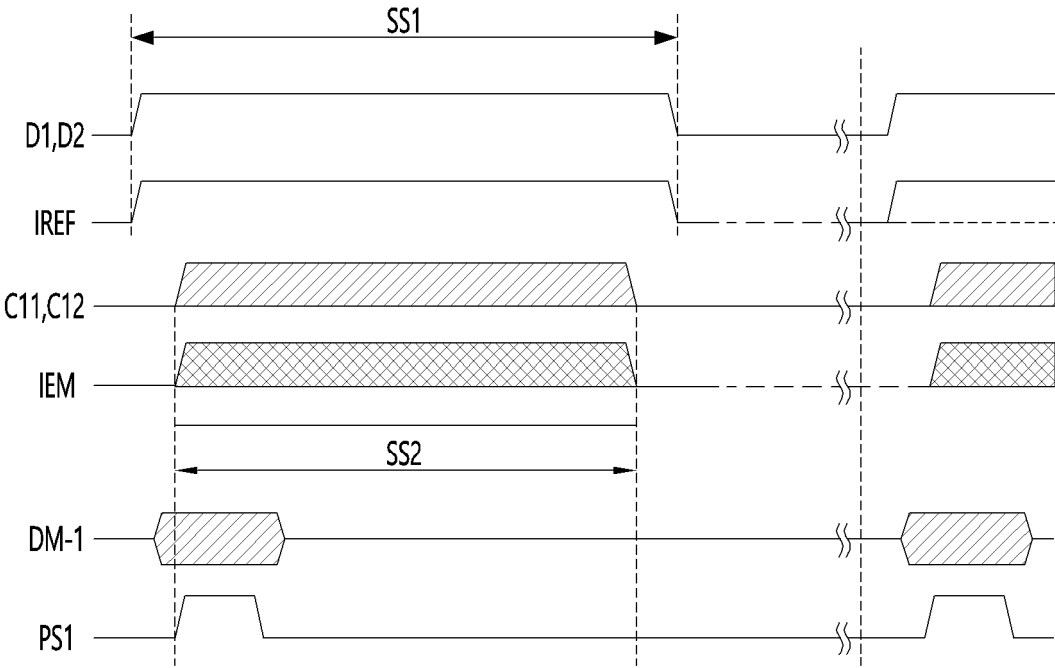


FIG. 17



INTERNATIONAL SEARCH REPORT

International application No.

PCT/KR2024/012739

A. CLASSIFICATION OF SUBJECT MATTER**G09G 3/32**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G 3/32(2006.01); G09G 3/20(2006.01); G09G 3/30(2006.01); H05B 45/325(2020.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models: IPC as above

Japanese utility models and applications for utility models: IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS (KIPO internal) & keywords: 기준 전류(reference current), 정 전류(constant current), 서브픽셀(sub-pixel), 트랜지스터(transistor), 미러(mirror), PWM(pulse width modulation)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR 10-2023-0013608 A (SAMSUNG ELECTRONICS CO., LTD.) 26 January 2023 (2023-01-26) See paragraphs [0195], [0201], [0472] and [0883]; claims 1 and 9; and figures 14 and 38-39a.	1-18
Y	KR 10-0742063 B1 (CASIO COMPUTER CO., LTD.) 23 July 2007 (2007-07-23) See paragraphs [0036] and [0046]-[0047]; and figure 2.	1-18
Y	KR 10-0480723 B1 (LG ELECTRONICS INC.) 07 April 2005 (2005-04-07) See paragraphs [0014]-[0016]; claim 1; and figure 1.	3,7-18
Y	KR 10-0884679 B1 (SEIKO INSTRUMENTS INC.) 18 February 2009 (2009-02-18) See paragraphs [0028], [0031] and [0069]; and figure 1.	13-18
A	KR 10-2007-0031897 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 20 March 2007 (2007-03-20) See paragraphs [0020]-[0025]; and figure 1.	1-18

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

02 December 2024

Date of mailing of the international search report

02 December 2024

Name and mailing address of the ISA/KR

Korean Intellectual Property Office**Government Complex-Daejeon Building 4, 189 Cheongsaro, Seo-gu, Daejeon 35208**Facsimile No. **+82-42-481-8578**

Authorized officer

Telephone No.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/KR2024/012739

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